**( V ) Preliminary Specifications**
**( ) Final Specifications**

| | |
|---|---|
| **Module** | **12.5”(12.5”) HD 16:9 Color TFT-LCD with LED Backlight design** |
| **Model Name** | **B125XTN03.0** |
| **Note ( )** | ***LED Backlight with driving circuit design*** |

| | |
|---|---|
| **Customer** | **Date** |
| **Checked & Approved by** | **Date** |
| Note: This Specification is subject to change without notice. | |

| | |
|---|---|
| **Approved by** | **Date** |
| Grace Hung | 2015/06/03 |
| **Prepared by** | **Date** |
| Christine Huang | 2015/06/03 |
| **NBBU Marketing Division AU Optronics corporation** | |

# Contents

# Record of Revision

| Version and Date | Page | Old description | New Description | Remark |
|---|---|---|---|---|
| 0.1 2015/03/19 | All | First Edition for Customer | | |
| 0.2 2015/06/03 | 5 | Power Consumption: TBD | Power Consumption:4.3Max | |
| | 11 | 3. Funcitonal Block Diagram | Update funcitonal block diagram | |
| | 12 | 4.1 Absolute Ratings of TFT LCD Module | Update Absolute Ratings of TFT LCD Module | |
| | 13 | 5.1.1 Power Specificaiton | Update Power Specificaiton | |
| | 14 | 5.1.2 Signal Eletrical Characteristics: VDD | 5.1.2 Signal Eletrical Characteristics: VDD>LCDVCC | |
| | 16 | 5.2 Backlight Unit | Update LED Characteristics and Backlight input signal characteristics | |
| | 19 | 6.2.2 Pin Assignment | Update Pin Assignment | |
| | 20 | 6.2.2 Pin Assignment Diagram | Update Pin Assignment Diagram | |
| | 21 | 6.3.1 Timing Charateristics: Frame Rate Symbol:- | 6.3.1 Timing Charateristics: Frame Rate Symbol:F | |
| | 23 | 6.4 Power On/off Sequence | Update Power on/off sequence note LCDVDD>LCDVCC | |
| | 24 | Display Port panel B/L power sequence timing parameter | Update Dsplay Port panel B/L power sequence timing parameter diagram | |
| | 25 | 7.1 Reliability Test | Update Reliability test table | |
| | 26 | 8.1 LCM Outline Dimension | Update LCM outline dimension drawing | |
| | 28 | 9.1 Shipping Label Format | Update Shipping Label format | |

## 1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

## 2. General Description

B125XTN03.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B125XTN03.0 is designed for a display unit of notebook style personal computer and industrial machine.

## 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

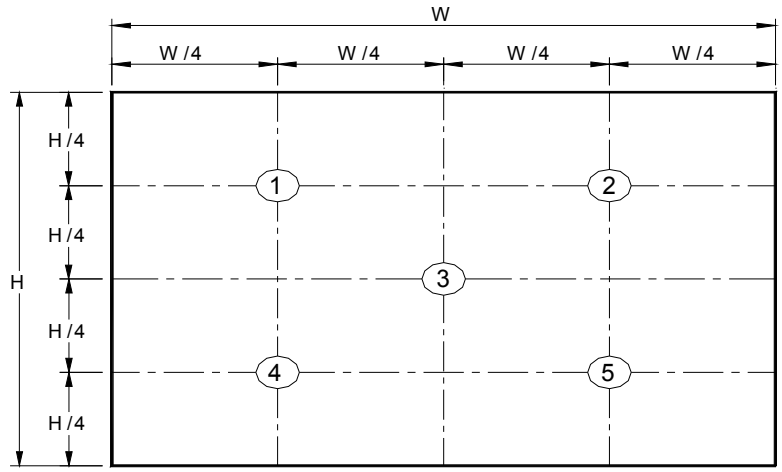
| Items | Unit | Specifications | | | |
|---|---|---|---|---|---|
| Screen Diagonal | [mm] | 317.3 | | | |
| Active Area | [mm] | 276.615 x 155.52 | | | |
| Pixels H x V | | 1366x3(RGB) x 768 | | | |
| Pixel Pitch | [mm] | 0.2025x0.2025 | | | |
| Pixel Format | | R.G.B. Vertical Stripe | | | |
| Display Mode | | Normally White | | | |
| White Luminance ($I_{LED}$=25mA) **(Note: ILED is LED current)** | [cd/m$^2$] | 300 typ. (5 points average)<br>240 min. (5 points average) | | | |
| Luminance Uniformity | | 1.25 max. (5 points) | | | |
| Contrast Ratio | | 400 typ | | | |
| Response Time | [ms] | 16 typ / 25 Max | | | |
| Nominal Input Voltage LCDVCC | [Volt] | +3.3 typ. | | | |
| Power Consumption | [Watt] | 4.3 max. | | | |
| Weight | [Grams] | 250 max. | | | |
| Physical Size **Include bracket** | [mm] | | Min. | Typ. | Max. |
| | | Length | 290.0 | 290.5 | 291.0 |
| | | Width | 180.9 | 181.4 | 181.9 |
| | | Thickness | - | - | 3.0 |
| Electrical Interface | | 1 Lane eDP1.2 | | | |
| Glass Thickness | [mm] | 0.4 | | | |
| Surface Treatment | | Anti Glare | | | |
| Support Color | | 262K colors ( RGB 6-bit ) | | | |
| Temperature Range<br>Operating<br>Storage (Non-Operating) | <br>[°C]<br>[°C] | <br>0 to +50<br>-20 to +60 | | | |
| RoHS Compliance | | RoHS Compliance | | | |

## 2.2 Optical Characteristics

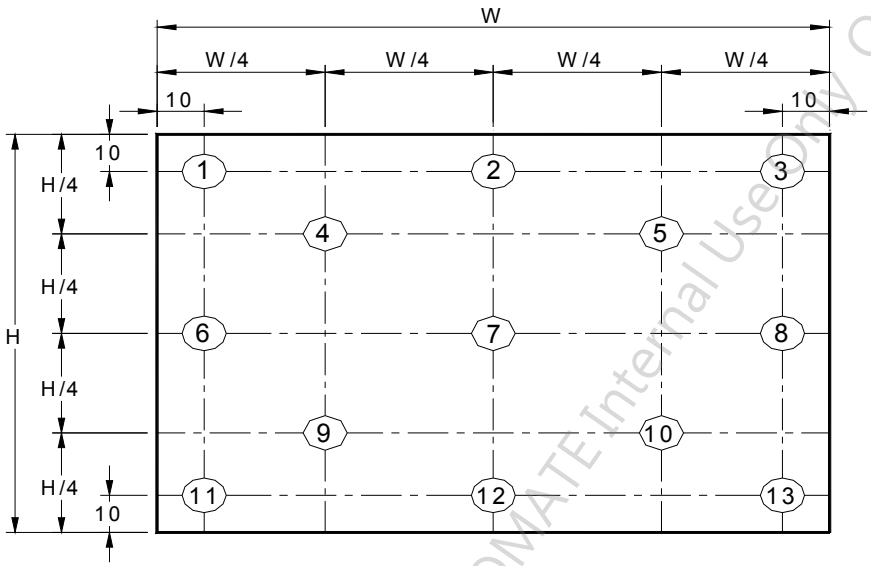
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

| Item | | Symbol | Conditions | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| White Luminance $I_{LED}$=25mA | | | 5 points average | 240 | 300 | - | cd/m$^2$ | 1, 4, 5. |
| Viewing Angle | | $\theta_R$ | Horizontal (Right) CR = 10 | 60 | 70 | - | degree | 4, 9 |
| | | $\theta_L$ | (Left) | 60 | 70 | - | | |
| | | $\psi_H$ | Vertical (Upper) CR = 10 | 45 | 55 | - | | |
| | | $\psi_L$ | (Lower) | 55 | 65 | - | | |
| Luminance Uniformity | | $\delta_{5P}$ | 5 Points | - | - | 1.25 | | 1, 3, 4 |
| Luminance Uniformity | | $\delta_{13P}$ | 13 Points | - | - | 1.53 | | 2, 3, 4 |
| Contrast Ratio | | CR | | 300 | 400 | - | | 4, 6 |
| Cross talk | | % | | | | 4 | | 4, 7 |
| Response Time | | $T_{RT}$ | Rising + Falling | - | 16 | 25 | msec | 4, 8 |
| Color / Chromaticity Coodinates | Red | Rx | CIE 1931 | TBD | TBD | TBD | | 4 |
| | | Ry | | TBD | TBD | TBD | | |
| | Green | Gx | | TBD | TBD | TBD | | |
| | | Gy | | TBD | TBD | TBD | | |
| | Blue | Bx | | TBD | TBD | TBD | | |
| | | By | | TBD | TBD | TBD | | |
| | White | Wx | | TBD | TBD | TBD | | |
| | | Wy | | TBD | TBD | TBD | | |
| NTSC | | % | | - | 45 | - | | |

**Note 1**: 5 points position (Ref: Active area)




**Note 2**: 13 points position (Ref: Active area)




**Note 3**: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

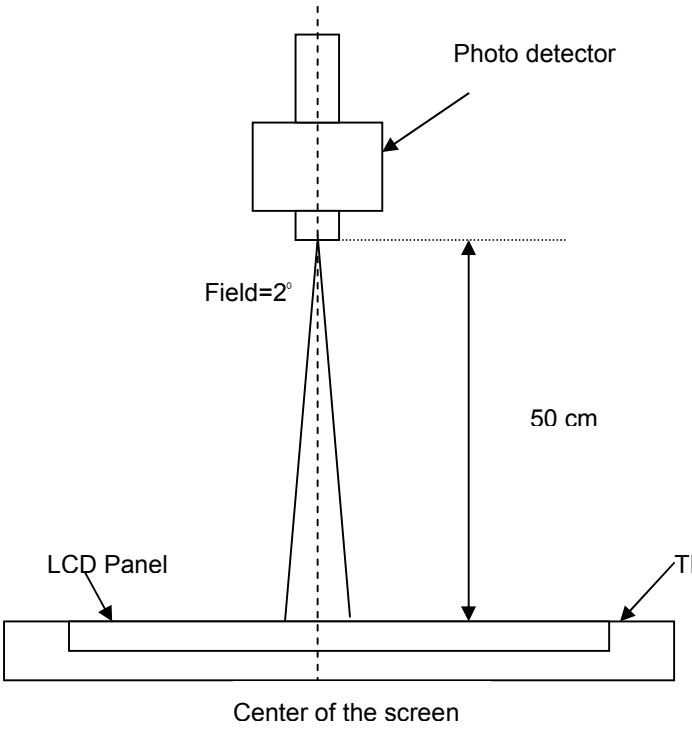
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

**Note 4**: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.




**Note 5** : Definition of Average Luminance of White ($Y_L$):

Measure the luminance of gray level 63 at 5 points , $Y_L$ = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

**Note 6** : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

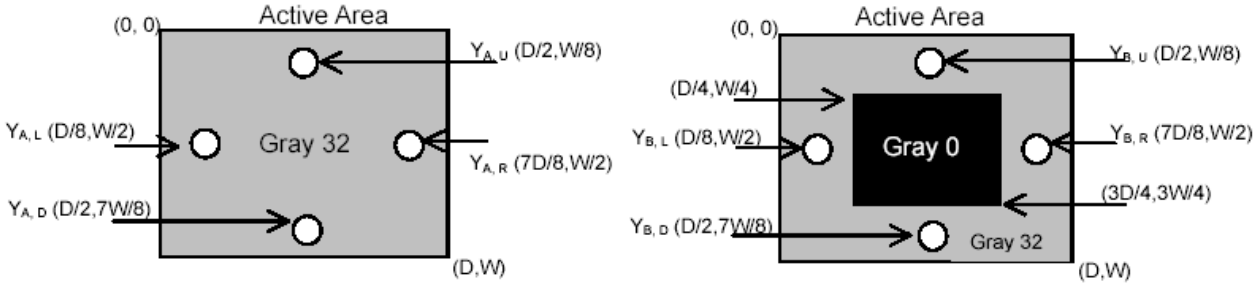
**Note 7** : Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

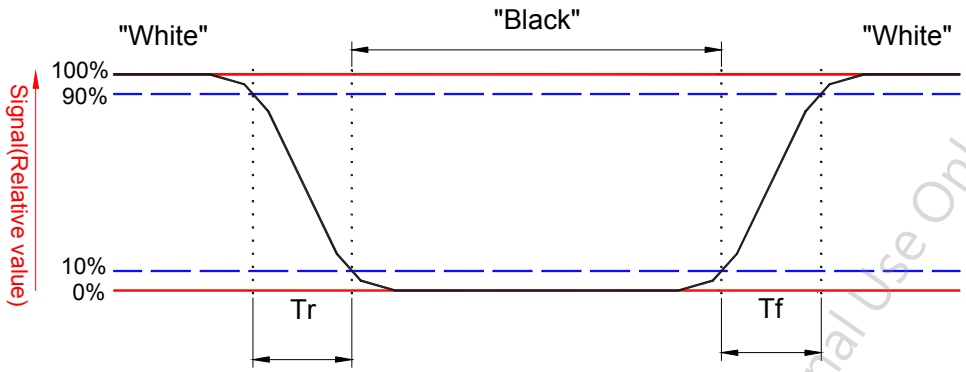
$Y_A$ = Luminance of measured location without gray level 0 pattern (cd/m2)

$Y_B$ = Luminance of measured location with gray level 0 pattern (cd/m2)



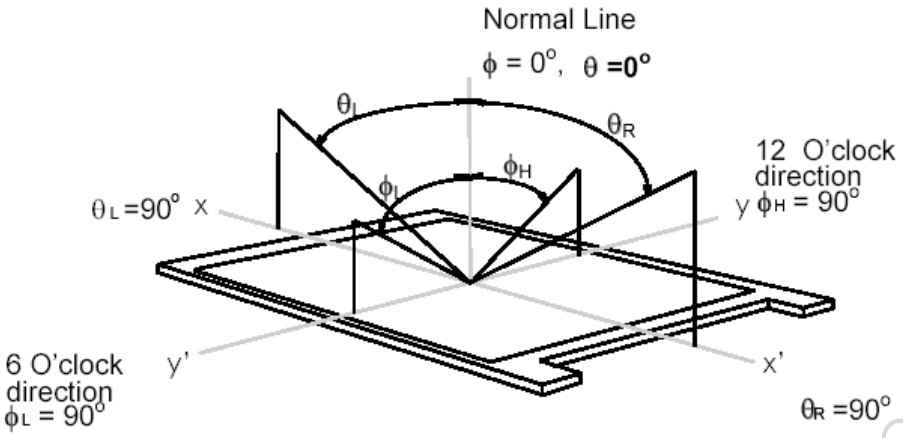

**Note 8**: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



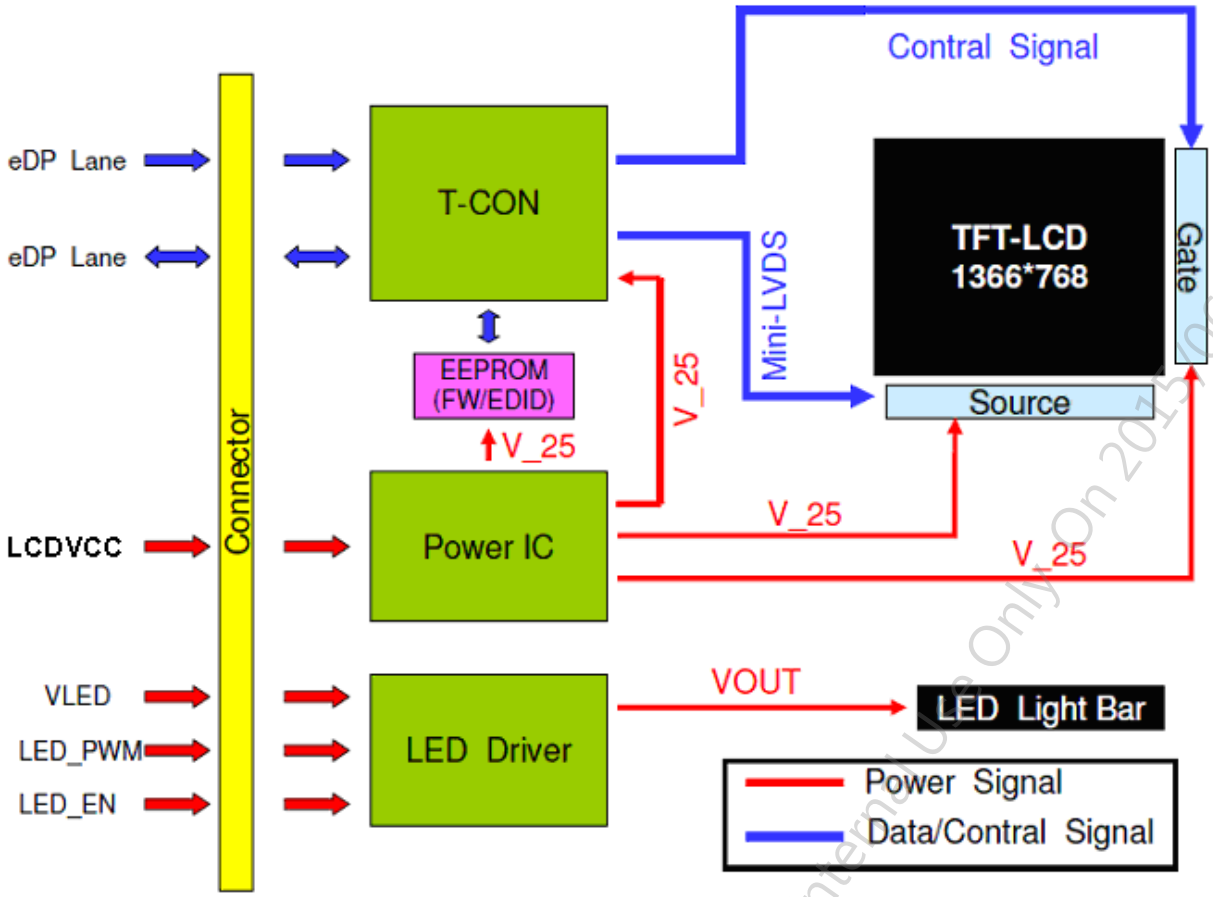
**Note 9**. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## 3. Functional Block Diagram

The following diagram shows the functional block of the 12.5 inches wide Color TFT/LCD 30 Pin



# 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

## 4.1 Absolute Ratings of TFT LCD Module

| Item | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Logic/LCD Drive Voltage | $V_{LCDVCC}$ | -0.3 | +4.0 | [Volt] | Note 1,2 |
| Converter Input Voltage | VLED | -0.3 | 23 | [Volt] | Note 1,2 |
| Converter Control Signal | $V_{LED\_PWM}$ | -0.3 | 6 | [Volt] | Note 1,2 |
| Converter Control Signal | $V_{LED\_EN}$ | -0.3 | 6 | [Volt] | Note 1,2 |

## 4.2 Absolute Ratings of Environment

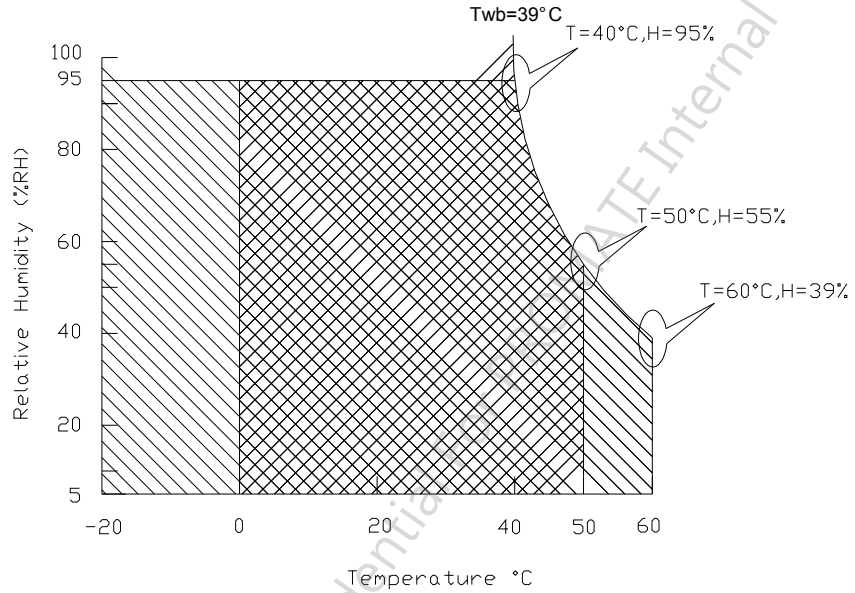
| Item | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Operating Temperature | TOP | 0 | +50 | [°C] | Note 4 |
| Operation Humidity | HOP | 5 | 95 | [%RH] | Note 4 |
| Storage Temperature | TST | -20 | +60 | [°C] | Note 4 |
| Storage Humidity | HST | 5 | 95 | [%RH] | Note 4 |

Note 1: At Ta (25°C )

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).




Operating Range Storage Range +

# 5. Electrical Characteristics

## 5.1 TFT LCD Module

### 5.1.1 Power Specification

Input power specifications are as follows;

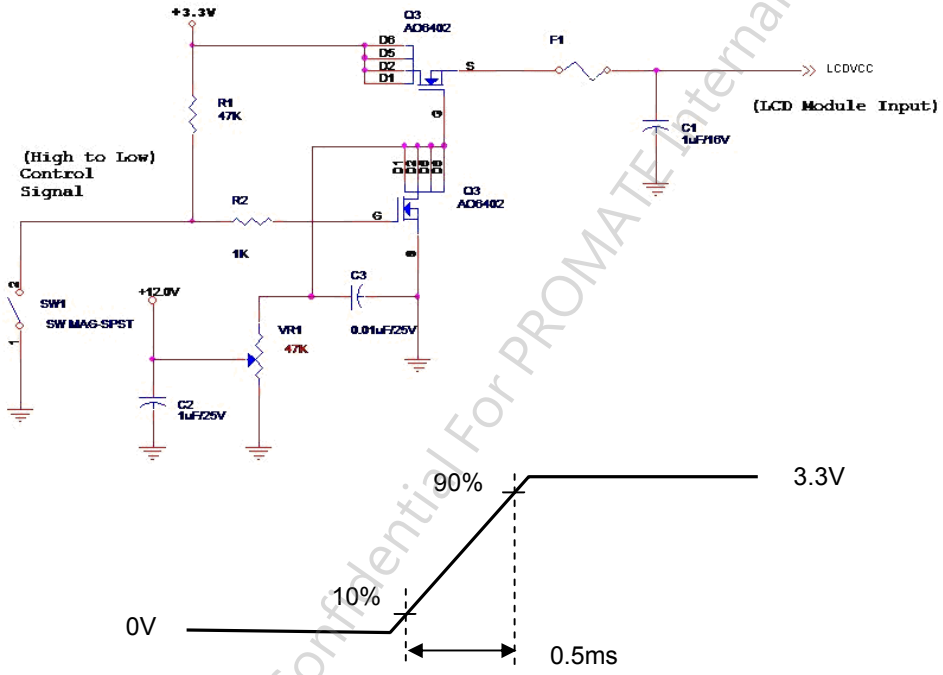
The power specification are measured under 25°C and frame frenquency under 60Hz

| Symbol | Parameter | Min | Typ | Max | Units | Note |
|---|---|---|---|---|---|---|
| LCDVCC | Logic/LCD Drive Voltage | 3.0 | 3.3 | 3.6 | [Volt] | |
| $P_{LCDVCC}$ | LCDVCC Power | _ | - | 1.1 | [Watt] | Note 1 |
| $I_{LCDVCC}$ | LCDVCC Current | _ | _ | 333 | [mA] | Note 1 |
| $I_{Rush}$ | Inrush Current | - | - | 1500 | [mA] | Note 2 |
| $LCDVCC_{rp}$ | Allowable Logic/LCD Drive Ripple Voltage | - | - | 100 | [mV] p-p | |

Note 1 : Maximum Measurement Condition：Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Typical Measurement Condition : Mosaic Pattern

Note 2：Measure Condition



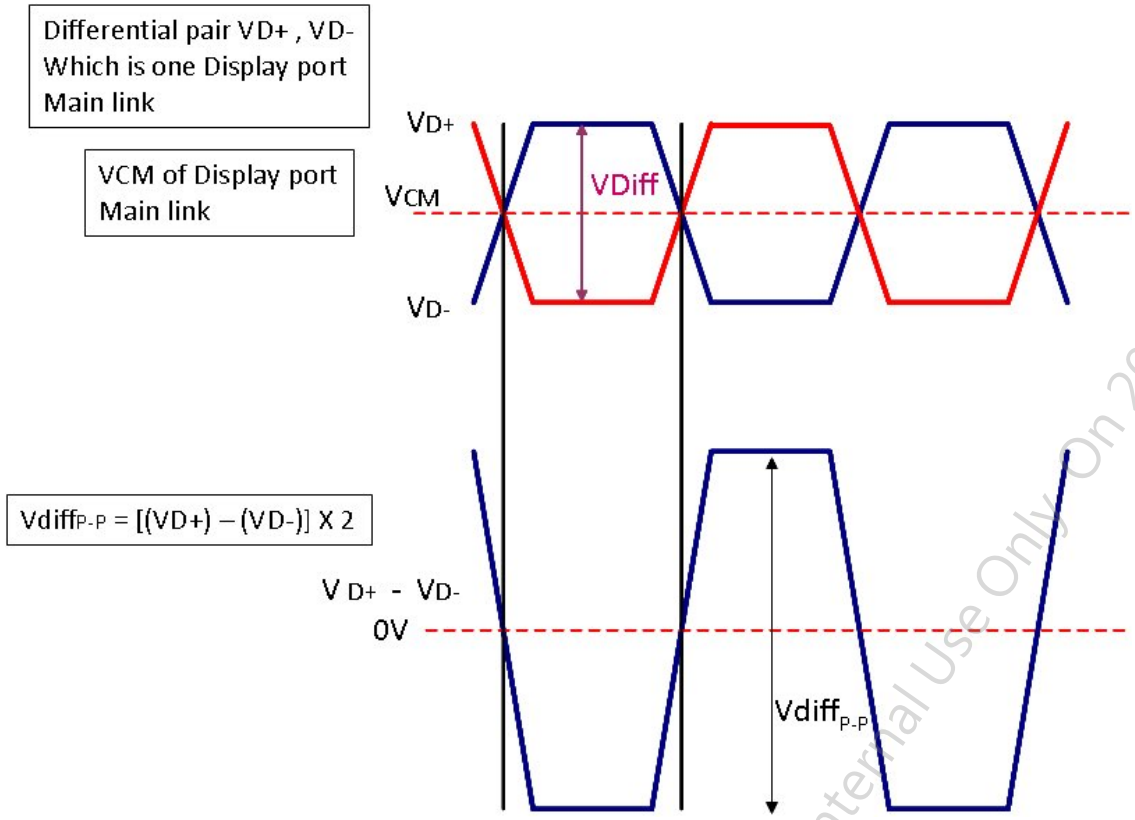

**LVDVCC rising time**

### 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when LCDVCC is off.

Signal electrical characteristics are as follows;

**Display Port main link signal:**

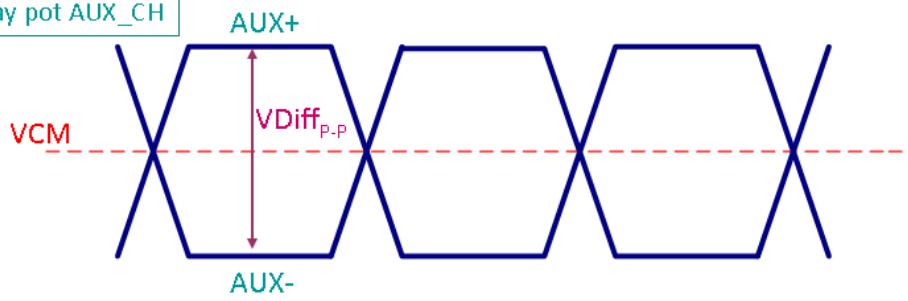



| Display port main link | | | | | |
|---|---|---|---|---|---|
| | | Min | Typ | Max | unit |
| VCM | RX input DC Common Mode Voltage | | 0 | | V |
| $VDiff_{P-P}$ | Peak-to-peak Voltage at a receiving Device | 100 | | 1320 | mV |

Follow as VESA display port standard V1.2

## Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display pot AUX_CH




| Display port AUX_CH | | | | | |
|---|---|---|---|---|---|
| | | Min | Typ | Max | unit |
| VCM | AUX DC Common Mode Voltage | | 0 | | V |
| $VDiff_{P-P}$ | AUX Peak-to-peak Voltage at a receiving Device | 0.4 | 0.6 | 0.8 | V |

Follow as VESA display port standard.

## Display Port $V_{HPD}$ signal:

| Display port VHPD | | | | | |
|---|---|---|---|---|---|
| | | Min | Typ | Max | unit |
| VHPD | HPD Voltage | 2.25 | | 3.6 | V |

Follow as VESA display port standard V1.2.

## 5.2 Backlight Unit

### 5.2.1 LED characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|
| Backlight Power Consumption | PLED | - | - | 3.2 | [Watt] | (Ta=25°C), Note 1 VLED =12V |
| LED Life-Time | N/A | 15,000 | - | - | Hour | (Ta=25°C), Note 2 $I_F$=25 mA |

**Note 1:** Calculator value for reference $P_{LED}$ = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

### 5.2.2 Backlight input signal characteristics

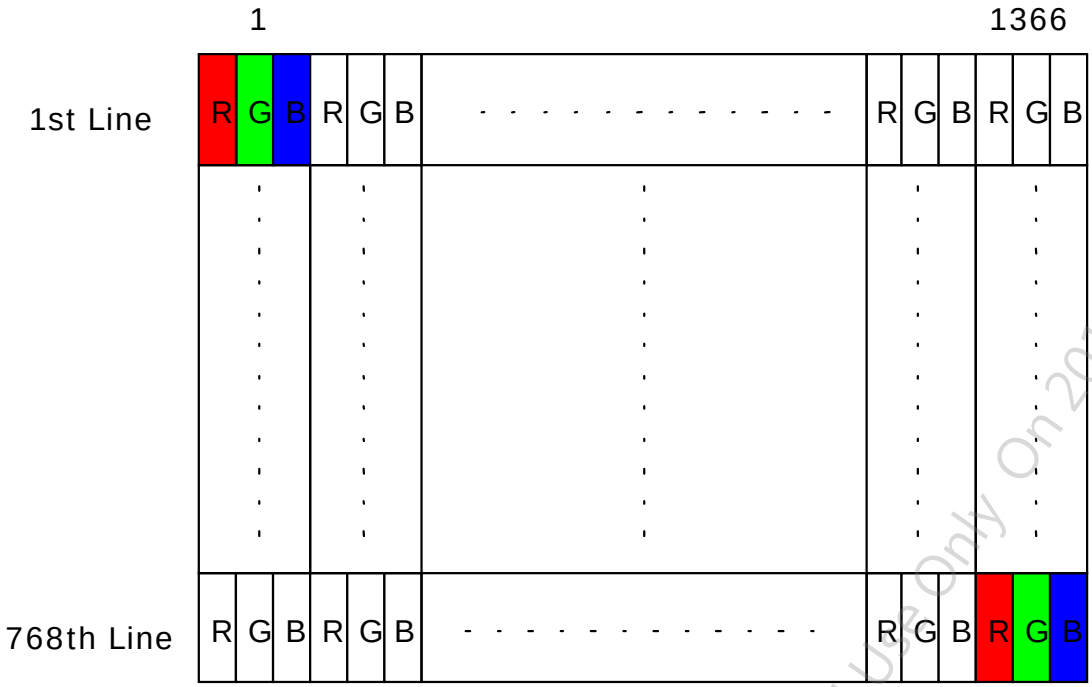
| Parameter | Symbol | Min | Typ | Max | Units | Remark |
|---|---|---|---|---|---|---|
| LED Power Supply | VLED | 5.0 | 12.0 | 21.0 | [Volt] | Define as Connector Interface (Ta=25°C) |
| Inrush Current | $I_{LEDRUSH}$ | - | - | 2 | [A] | |
| LED Enable Input High Level | $V_{LED\_EN}$ | 2.2 | - | 5.5 | [Volt] | |
| LED Enable Input Low Level | | - | - | 0.5 | [Volt] | |
| PWM Logic Input High Level | $V_{LED\_PWM}$ | 2.2 | - | 5.5 | [Volt] | |
| PWM Logic Input Low Level | | - | - | 0.5 | [Volt] | |
| PWM Input Frequency | $F_{LED\_PWM}$ | 200 | 1K | 10K | Hz | |
| PWM Duty Ratio | Duty | 5 | -- | 100 | % | |

**Note 1 :** Recommend system pull up/down resistor no bigger than 10kohm

# 6. Signal Interface Characteristic

## 6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



## 6.2 Integration Interface Requirement

### 6.2.1 Connector Description

Physical interface is described as for the connector on module.

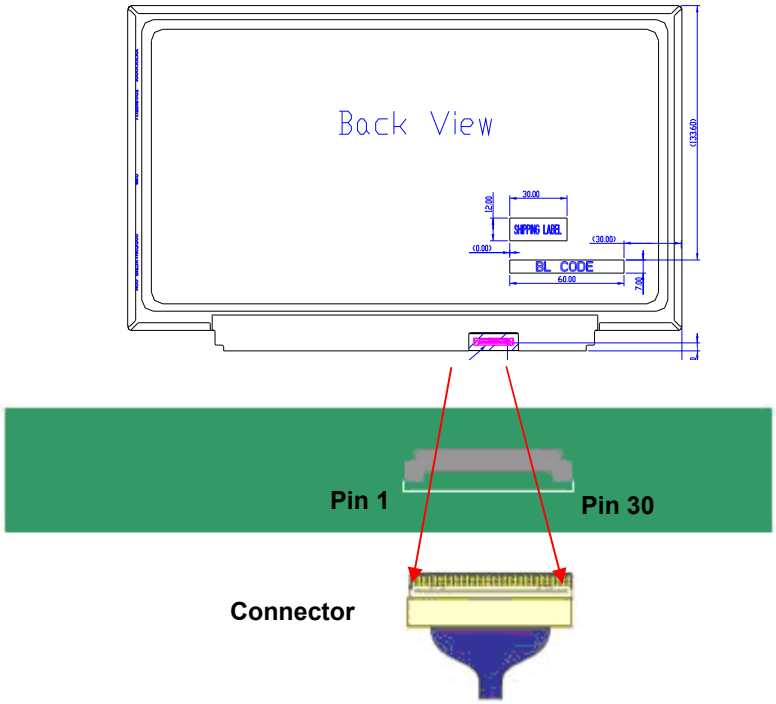
These connectors are capable of accommodating the following signals and will be following components.

| Connector Name / Designation | For Signal Connector |
|---|---|
| Manufacturer | HRS or Compatible |
| Type / Part Number | HRS KN38A-30S-0.5H or Compatible |
| Mating Housing/Part Number | IPEX 20353-030T-11 or Compatible |

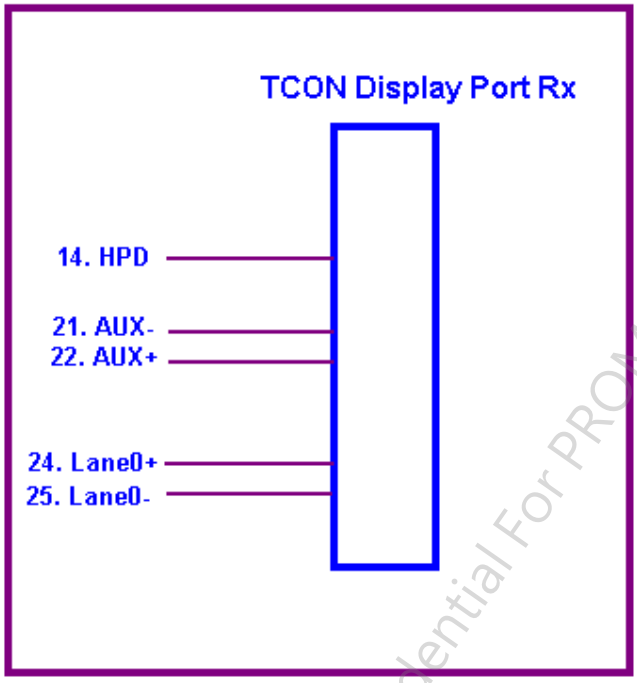
### 6.2.2 Pin Assignment (1 Lane)

**eDP lane** is a differential signal technology for LCD interface and high speed data transfer device.

| PIN# | Signal Name | Description |
|---|---|---|
| 1 | NC | No Connect (Reserved for CM) |
| 2 | VLED | Backlight power (6V~21V) |
| 3 | VLED | Backlight power (6V~21V) |
| 4 | VLED | Backlight power (6V~21V) |
| 5 | VLED | Backlight power (6V~21V) |
| 6 | NC | No connect (Reverse for AUO TEST only) |
| 7 | H_SYNC or NC | H_SYNC function(Optional) or NC |
| 8 | LED_PWM | System PWM signal Input |
| 9 | LED_EN | Backlight On / Off |
| 10 | BL_GND | Backlight ground |
| 11 | BL_GND | Backlight ground |
| 12 | BL_GND | Backlight ground |
| 13 | BL_GND | Backlight ground |
| 14 | HPD | HPD signal pin |
| 15 | LCDGND | LCD logic and driver ground |
| 16 | LCDGND | LCD logic and driver ground |
| 17 | LCD_Self_Test or NC | LCD Panel Self Test Enable (Optional) |
| 18 | LCDVCC | LCD logic and driver power |
| 19 | LCDVCC | LCD logic and driver power |
| 20 | H_GND | High Speed Ground |
| 21 | AUX_CH_N | Comp Signal Auxiliary Ch. |
| 22 | AUX_CH_P | True Signal Auxiliary Ch. |
| 23 | H_GND | High Speed Ground |
| 24 | Lane0_P | True Signal Link Lane 0 |
| 25 | Lane0_N | Comp Signal Link Lane 0 |
| 26 | H_GND | High Speed Ground |
| 27 | Lane1_P | True Signal Link Lane 1 |
| 28 | Lane1_N | Comp Signal Lane 1 |
| 29 | H_GND | High Speed Ground |
| 30 | NC | No Connect (Reserved for DCR) |




**Note1:** Start from right side.
**Note2:** Input signals shall be low or High-impedance state when LCDVCC is off.
Internal circuit of **eDP inputs** are as following.



## 6.3 Interface Timing

### 6.3.1 Timing Characteristics

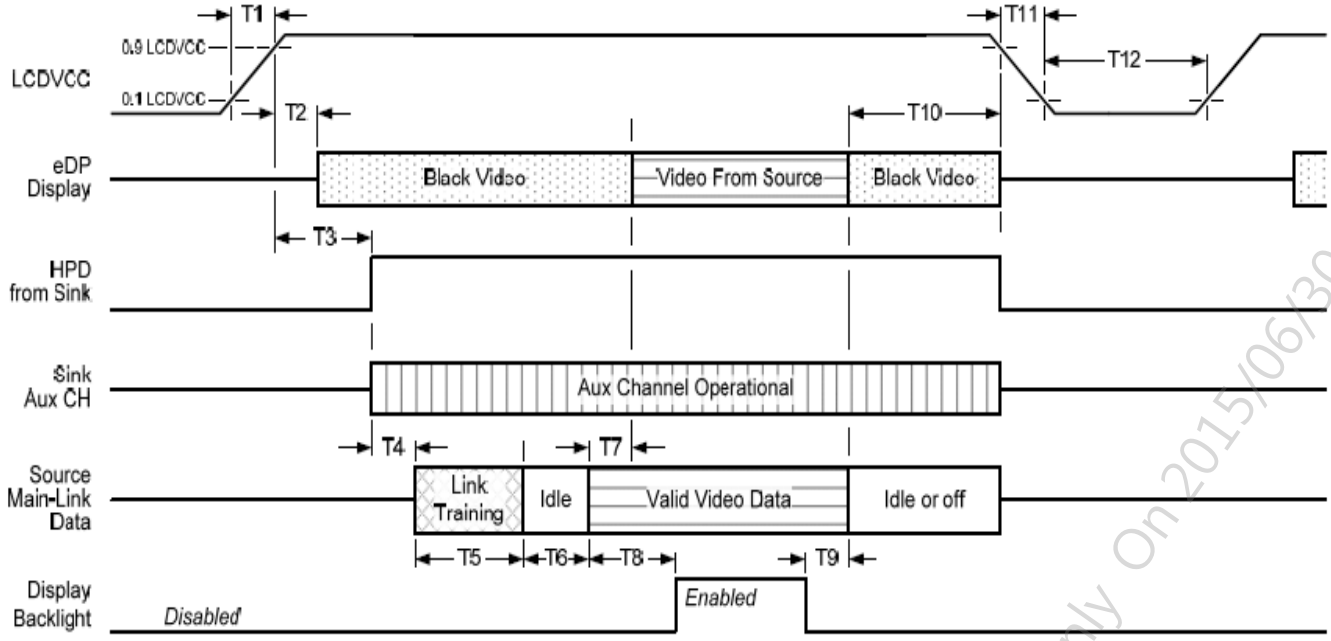
Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Frame Rate | | F | - | 60 | - | Hz |
| Clock frequency | | 1/ $T_{Clock}$ | 66.6 | 75.6 | 80 | MHz |
| Vertical Section | Period | $T_V$ | 788 | 790 | 768+A | $T_{Line}$ |
| | Active | $T_{VD}$ | 768 | | | |
| | Blanking | $T_{VB}$ | 20 | 22 | A | |
| Horizontal Section | Period | $T_H$ | 1416 | 1592 | 1366+B | $T_{Clock}$ |
| | Active | $T_{HD}$ | 1366 | | | |
| | Blanking | $T_{HB}$ | 50 | 226 | B | |

**Note 1 :** DE mode only
**Note 2 :** The maximum clock frequency = (1366+B)*(768+A)*60<80MHz

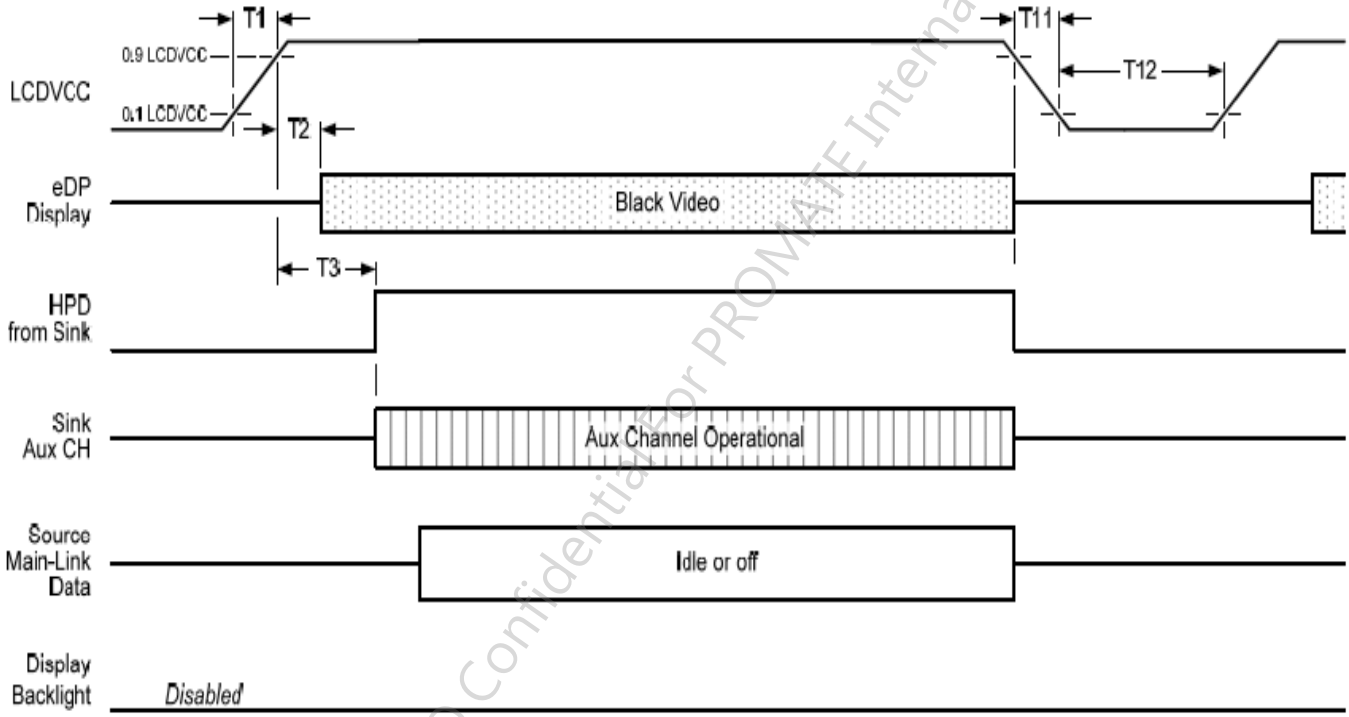
## 6.4 Power ON/OFF Sequence

**Display Port panel power sequence:**




**Display port interface power up/down sequence, normal system operation**

**Display Port AUX_CH transaction only:**




**Display port interface power up/down sequence, AUX_CH transaction only**

**Display Port panel power sequence timing parameter:**

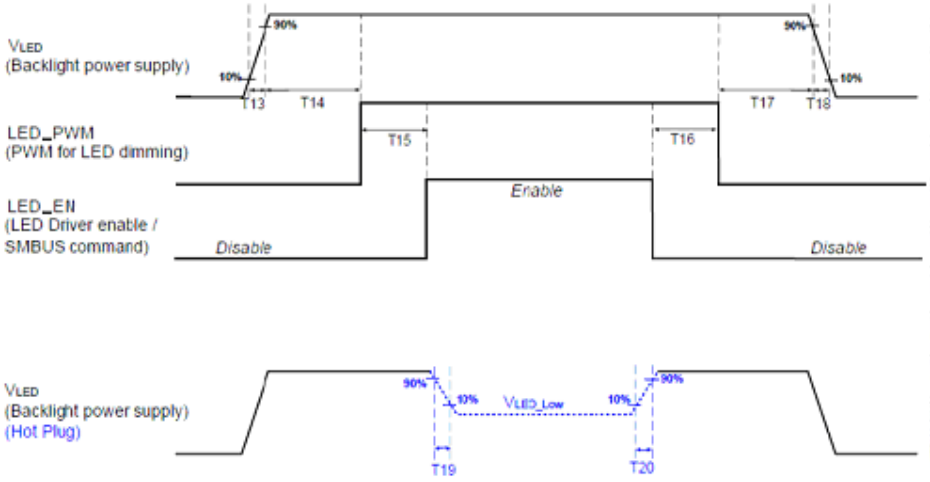
| Timing parameter | Description | Reqd. by | Limits | | | Notes |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| T1 | power rail rise time, 10% to 90% | source | 0.5ms | | 10ms | |
| T2 | delay from LCDVCCto black video generation | sink | 0ms | | 200ms | prevents display noise until valid video data is received from the source |
| T3 | delay from LCDVCCto HPD high | sink | 0ms | | 200ms | sink AUX_CH must be operational upon HPD high. |
| T4 | delay from HPD high to link training initialization | source | | | | allows for source to read link capability and initialize. |
| T5 | link training duration | source | | | | dependant on source link to read training protocol. |
| T6 | link idle | source | | | | Min accounts for required BS-Idle pattern.<br>Max allows for source frame synchronization. |
| T7 | delay from valid video data from source to video on display | sink | 0ms | | 50ms | max allows sink validate video data and timing. |
| T8 | delay from valid video data from source to backlight enable | source | | | | source must assure display video is stable. |
| T9 | delay from backlight disable to end of valid video data | source | | | | source must assure backlight is no longer illuminated. |
| T10 | delay from end of valid video data from source to power off | source | 0ms | | 500ms | |
| T11 | power rail fall time, 905 to 10% | source | | | 10ms | |
| T12 | power off time | source | 500ms | | | |

**Note1:** The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVCC power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

**Note 2:** The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

**Note 3:** The sink must support AUX_CH polling by the source immediately following LCDVCC power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

**Display Port panel B/L power sequence timing parameter:**




| | Min (ms) | Max (ms) |
|---|---|---|
| T13 | 0.5 | 10 |
| T14 | 10 | - |
| T15 | 0 | - |
| T16 | 0 | - |
| T17 | 10 | - |
| T18 | 0.5 | 10 |
| T19 | 1* | - |
| T20 | 1* | - |

Seamless change: T19/T20 = 5x$T_{PWM}$*

*$T_{PWM}$= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.

# 7. Panel Reliability Test

## 7.1 Reliability Test

Environment test conditions are listed as following table.

| Items | Required Condition | Note |
|---|---|---|
| Temperature Humidity Bias (THB) | Ta= 40 °C, 90%RH, 300hours | |
| High Temperature Operation (HTO) | Ta= 50 °C, 300hours | |
| Low Temperature Operation (LTO) | Ta= 0 °C, 300hours | |
| High Temperature Storage (HTS) | Ta= 60 °C, 300hours | |
| Low Temperature Storage (LTS) | Ta= -20 °C, 300hours | |
| Thermal Shock Test (TST) | -20 °C /30min, 60 °C /30min, 50 cycles | ***1*** |
| Vibration Test (Non-operation) | 0.025 g2/Hz, 10-500 Hz, nominal 3.5 grms 60min/direction, X,Y, Z 3directions | |
| Shock Test (Non-operation) | 240G,2ms, ±X, ±Y, ±Z, 6 directions | |
| Drop Test (package test) | Height: 610 mm, 1 corner, 3 edges, 6 flats | |
| Vibration Test (package test) | 1.5Grms, 10~200Hz, 30min./cycle, X,Y,Z 3directions | |
| On/Off Test | On/30sec, Off/30sec, 10,000 cycles | |
| ESD (Electro Static Discharge) | Contact Discharge: ± 8KV | ***2*** |
| | Air Discharge: ± 15KV | |

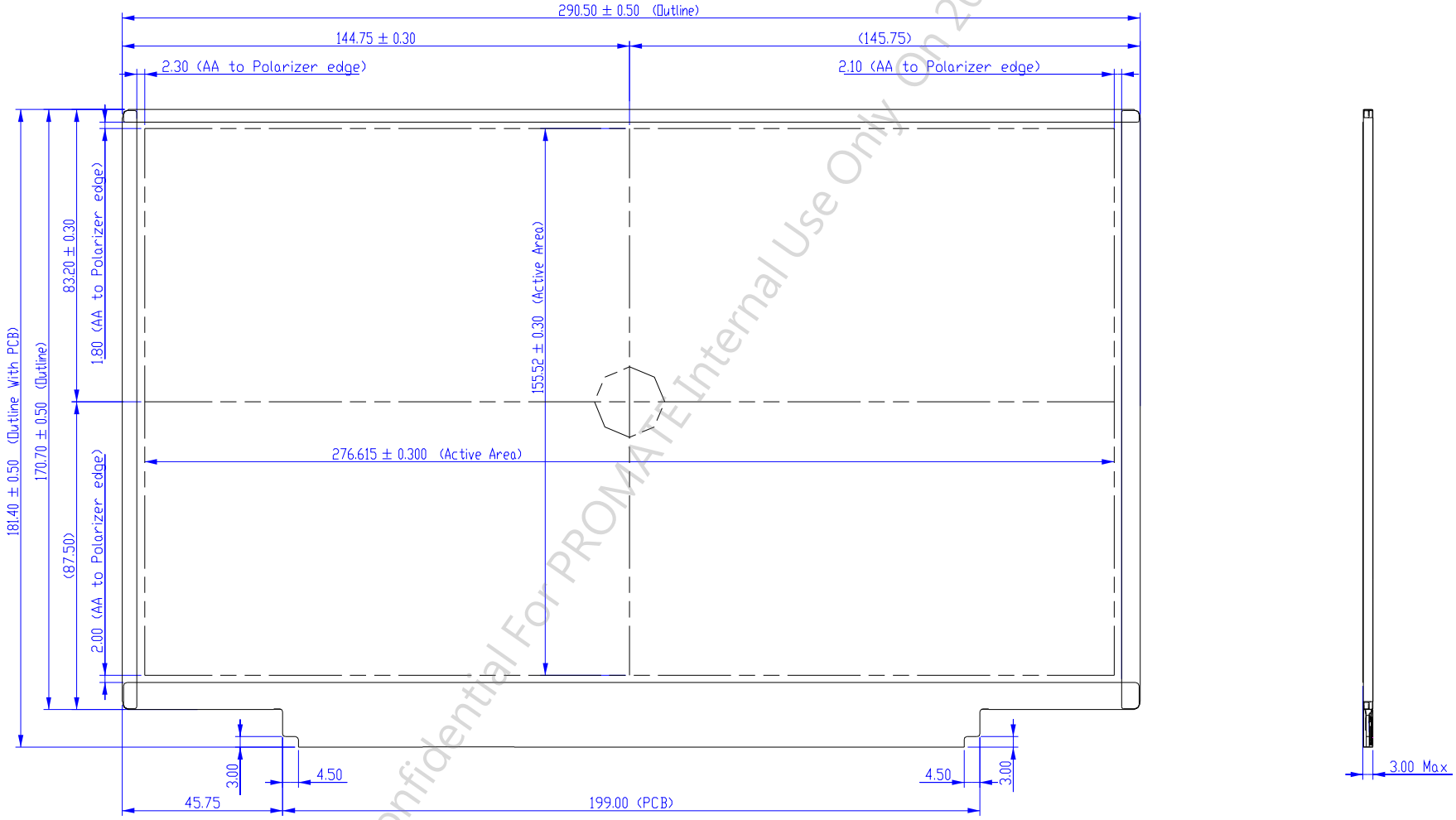
***Note 1***: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20 °C to 60 °C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

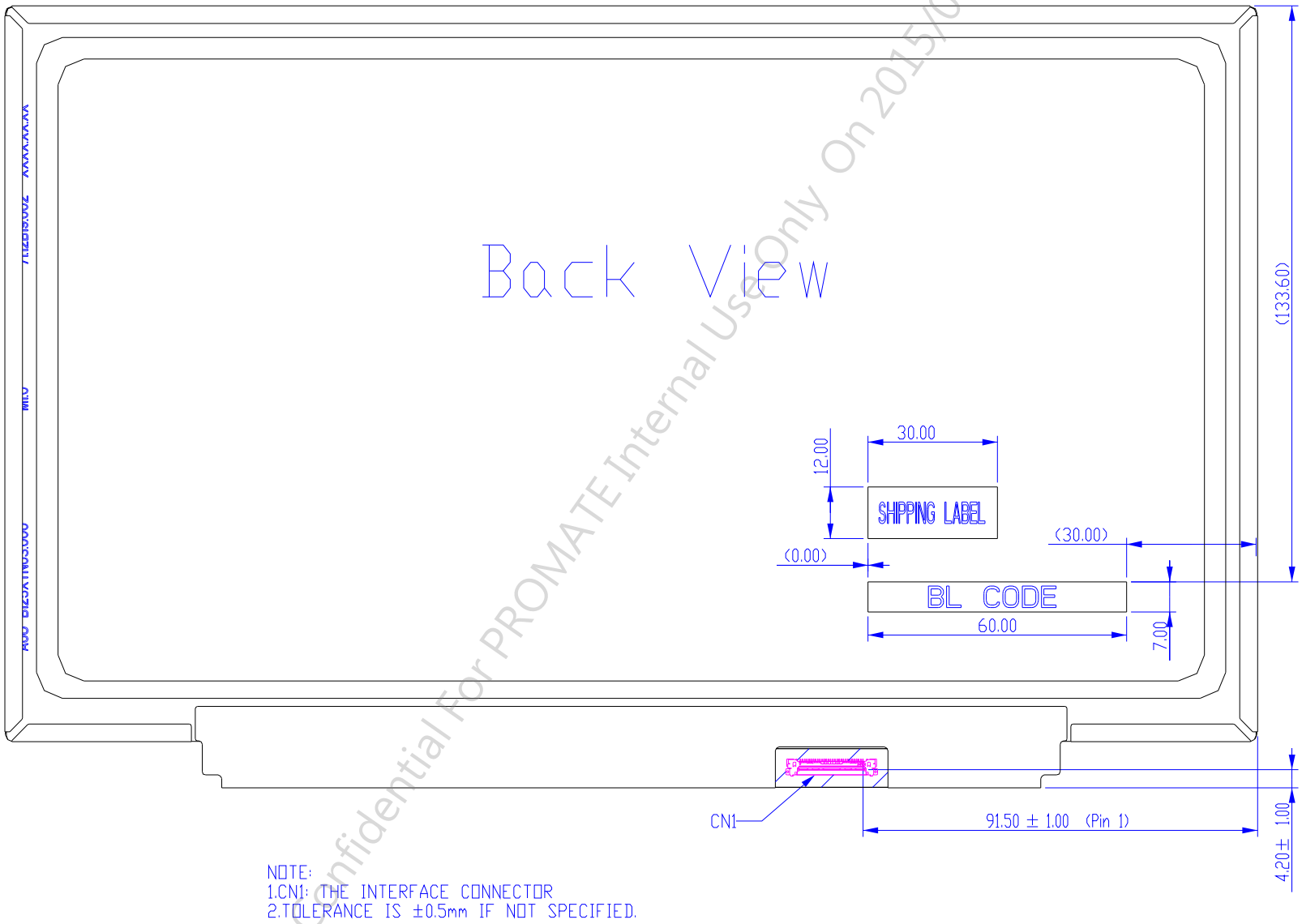
***Note 2***: EN61000-4-2, ESD class B: Certain performance degradation allowed No data los, Self-recoverable,

No hardware failures.

## 8. Mechanical Characteristics

### 8.1 LCM Outline Dimension

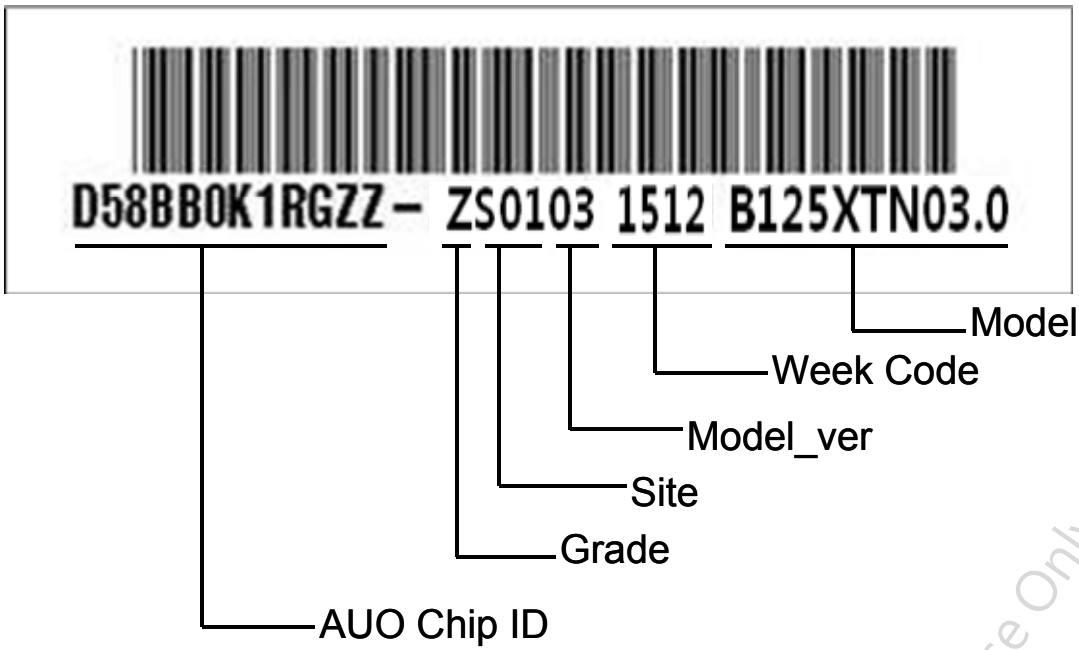




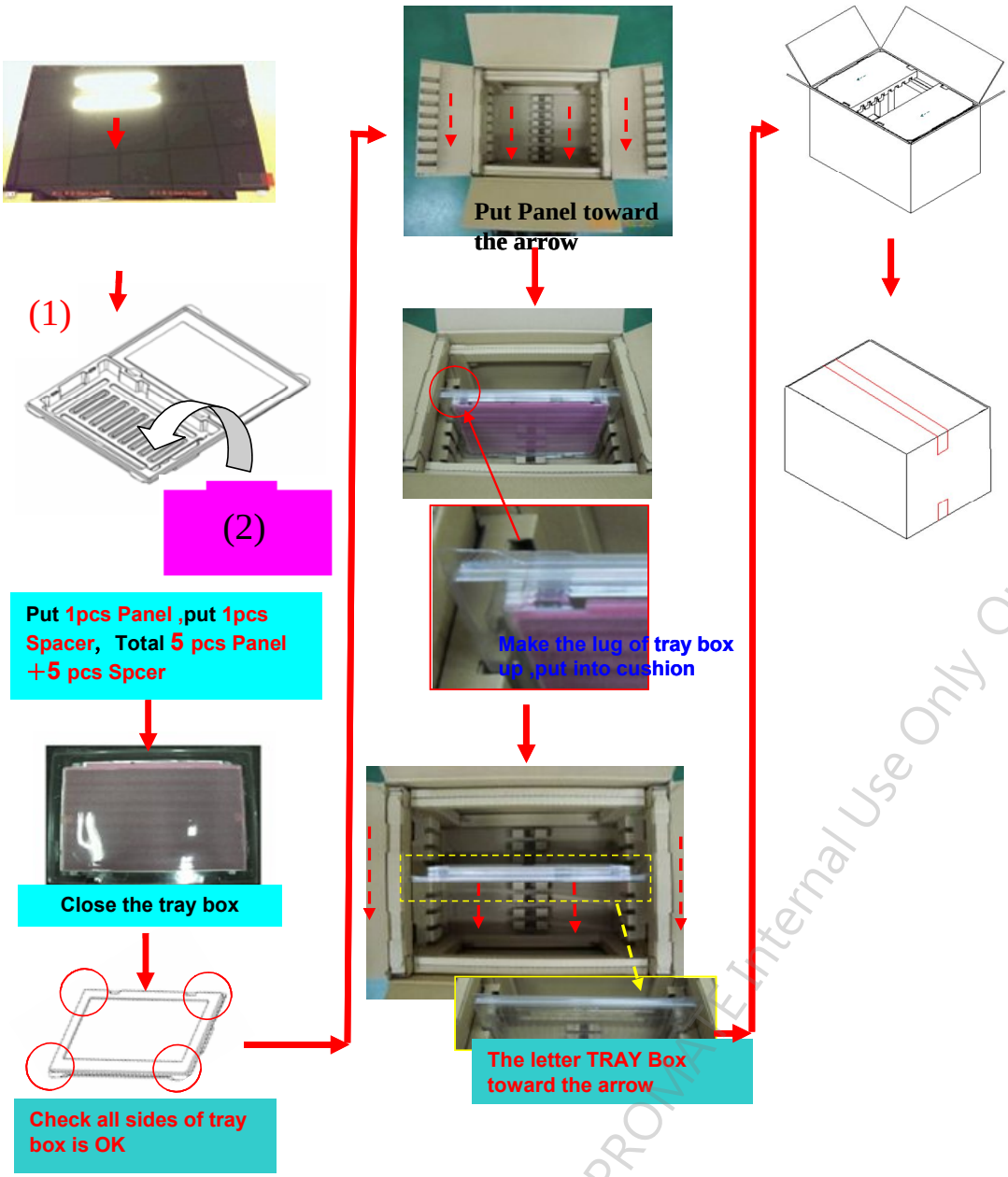

Note: Prevention IC damage, IC positions not allowed any overlap over these a

## 9. Shipping and Package

### 9.1 Shipping Label Format



## 9.2 Carton Package



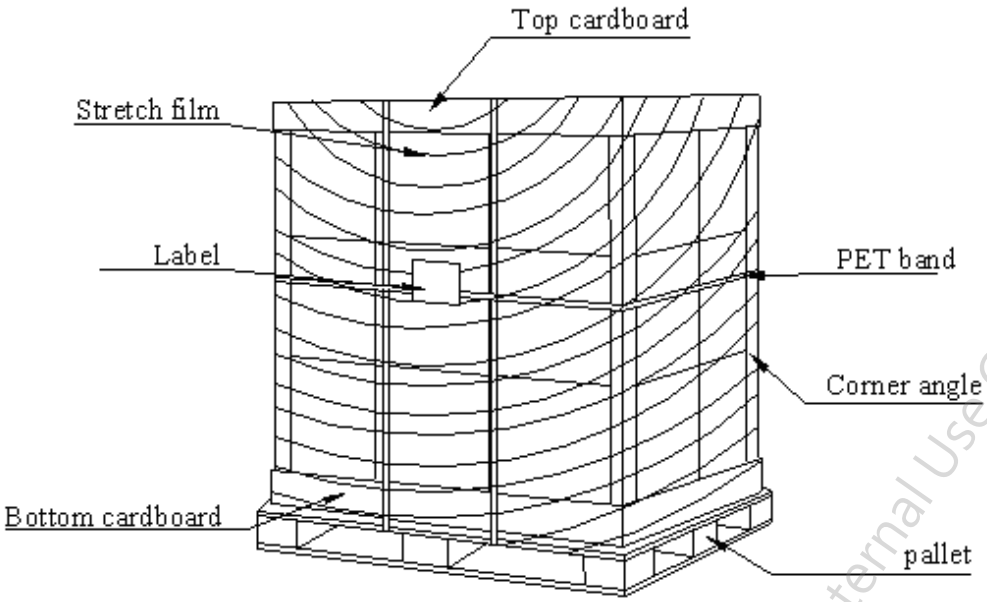

Max capacity：45 TFT-LCD module per carton

Outside dimension of carton:436mm(L)* 374mm(W)*273mm(H)

Pallet size： 1140 mm *890 mm * 132mm

## 9.3 Shipping Package of Palletizing Sequence

Module by air：(2 *3) *5 layers，one pallet put 30 boxes，total1350pcs module
Module by sea：(2 *3) *5 layers，one pallet put 30 boxes，total 1350pcs module
Module by sea_HQ：(2 *3) *5 layers，one pallet put 30 boxes，total 1350pcs module



## 10. Appendix: EDID Description

| Address | FUNCTION | Value | Value | Value | Note |
|---|---|---|---|---|---|
| HEX | | HEX | BIN | DEC | |
| 00 | Header | 00 | 00000000 | 0 | |
| 01 | | FF | 11111111 | 255 | |
| 02 | | FF | 11111111 | 255 | |
| 03 | | FF | 11111111 | 255 | |
| 04 | | FF | 11111111 | 255 | |
| 05 | | FF | 11111111 | 255 | |
| 06 | | FF | 11111111 | 255 | |
| 07 | | 00 | 00000000 | 0 | |
| 08 | EISA Manuf. Code LSB | 06 | 00000110 | 6 | |
| 09 | Compressed ASCII | AF | 10101111 | 175 | |
| 0A | Product Code | 6C | 01101100 | 108 | |
| 0B | hex, LSB first | 10 | 00010000 | 16 | |
| 0C | 32-bit ser # | 00 | 00000000 | 0 | |
| 0D | | 00 | 00000000 | 0 | |
| 0E | | 00 | 00000000 | 0 | |
| 0F | | 00 | 00000000 | 0 | |
| 10 | Week of manufacture | 00 | 00000000 | 0 | |
| 11 | Year of manufacture | 18 | 00011000 | 24 | |
| 12 | EDID Structure Ver. | 01 | 00000001 | 1 | |
| 13 | EDID revision # | 04 | 00000100 | 4 | |
| 14 | **Video input def.** *(digital I/P, non-TMDS, CRGB)* | 95 | 10010101 | 149 | |
| 15 | **Max H image size** *(rounded to cm)* | 1C | 00011100 | 28 | |
| 16 | **Max V image size** *(rounded to cm)* | 10 | 00010000 | 16 | |
| 17 | **Display Gamma** *(=(gamma*100)-100)* | 78 | 01111000 | 120 | |
| 18 | **Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)* | 02 | 00000010 | 2 | |
| 19 | Red/green low bits **(Lower 2:2:2:2 bits)** | BB | 10111011 | 187 | |
| 1A | Blue/white low bits **(Lower 2:2:2:2 bits)** | F5 | 11110101 | 245 | |
| 1B | Red x **(Upper 8 bits)** | 94 | 10010100 | 148 | |
| 1C | Red y/ highER 8 bits | 55 | 01010101 | 85 | |
| 1D | Green x | 54 | 01010100 | 84 | |
| 1E | Green y | 90 | 10010000 | 144 | |
| 1F | Blue x | 27 | 00100111 | 39 | |
| 20 | Blue y | 23 | 00100011 | 35 | |
| 21 | White x | 50 | 01010000 | 80 | |
| 22 | White y | 54 | 01010100 | 84 | |
| 23 | Established timing 1 | 00 | 00000000 | 0 | |
| 24 | Established timing 2 | 00 | 00000000 | 0 | |
| 25 | Established timing 3 | 00 | 00000000 | 0 | |
| 26 | Standard timing #1 | 01 | 00000001 | 1 | |
| 27 | | 01 | 00000001 | 1 | |
| 28 | Standard timing #2 | 01 | 00000001 | 1 | |
| 29 | | 01 | 00000001 | 1 | |
| 2A | Standard timing #3 | 01 | 00000001 | 1 | |
| 2B | | 01 | 00000001 | 1 | |

| | | | | | |
|---|---|---|---|---|---|
| **2C** | Standard timing #4 | 01 | 00000001 | 1 | |
| **2D** | | 01 | 00000001 | 1 | |
| **2E** | Standard timing #5 | 01 | 00000001 | 1 | |
| **2F** | | 01 | 00000001 | 1 | |
| **30** | Standard timing #6 | 01 | 00000001 | 1 | |
| **31** | | 01 | 00000001 | 1 | |
| **32** | Standard timing #7 | 01 | 00000001 | 1 | |
| **33** | | 01 | 00000001 | 1 | |
| **34** | Standard timing #8 | 01 | 00000001 | 1 | |
| **35** | | 01 | 00000001 | 1 | |
| **36** | Pixel Clock/10000 LSB | CE | 11001110 | 206 | |
| **37** | Pixel Clock/10000 USB | 1D | 00011101 | 29 | |
| **38** | Horz active **Lower 8bits** | 56 | 01010110 | 86 | |
| **39** | Horz blanking **Lower 8bits** | E2 | 11100010 | 226 | |
| **3A** | HorzAct:HorzBlnk **Upper 4:4 bits** | 50 | 01010000 | 80 | |
| **3B** | Vertical Active **Lower 8bits** | 00 | 00000000 | 0 | |
| **3C** | Vertical Blanking **Lower 8bits** | 1E | 00011110 | 30 | |
| **3D** | Vert Act : Vertical Blanking **(upper 4:4 bit)** | 30 | 00110000 | 48 | |
| **3E** | HorzSync. Offset | 26 | 00100110 | 38 | |
| **3F** | HorzSync.Width | 16 | 00010110 | 22 | |
| **40** | VertSync.Offset : VertSync.Width | 36 | 00110110 | 54 | |
| **41** | Horz&Vert Sync Offset/Width **Upper 2bits** | 00 | 00000000 | 0 | |
| **42** | Horizontal Image Size **Lower 8bits** | 15 | 00010101 | 21 | |
| **43** | Vertical Image Size **Lower 8bits** | 9C | 10011100 | 156 | |
| **44** | Horizontal & Vertical Image Size **(upper 4:4 bits)** | 10 | 00010000 | 16 | |
| **45** | Horizontal Border *(zero for internal LCD)* | 00 | 00000000 | 0 | |
| **46** | Vertical Border *(zero for internal LCD)* | 00 | 00000000 | 0 | |
| **47** | Signal *(non-intr, norm, no stero, sep sync, neg pol)* | 18 | 00011000 | 24 | |
| **48** | Pixel Clock/10,000 (LSB) | DF | 11011111 | 223 | |
| **49** | Pixel Clock/10,000 (MSB) | 13 | 00010011 | 19 | 40Hz frame rate |
| **4A** | Horizontal Addressable Pixels, lower 8 bits | 56 | 01010110 | 86 | |
| **4B** | Horizontal Blanking Pixels, lower 8 bits | E2 | 11100010 | 226 | |
| **4C** | H Pixels, upper nibble : H Blanking, upper nibble | 50 | 01010000 | 80 | |
| **4D** | Vertical Addressable Lines, lower 8 bits | 00 | 00000000 | 0 | |
| **4E** | Vertical Blanking Lines, lower 8 bits | 1E | 00011110 | 30 | |
| **4F** | V lines, upper nibble : V blanking, upper nibble | 30 | 00110000 | 48 | |
| **50** | Horizontal Front Porch, lower 8 bits | 26 | 00100110 | 38 | |
| **51** | Horizontal Sync Pulse, lower 8 bits | 16 | 00010110 | 22 | |
| **52** | V Front Porch, lower nibble : V Sync Pulse, lower nibble | 36 | 00110110 | 54 | |
| **53** | VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits | 00 | 00000000 | 0 | |
| **54** | Horizontal Image Size in mm, lower 8 bits | 15 | 00010101 | 21 | |
| **55** | Vertical Image Size in mm, lower 8 bits | 9C | 10011100 | 156 | |
| **56** | H Image Size, upper nibble : V Image Size, upper nibble | 10 | 00010000 | 16 | |
| **57** | Horizontal Border | 00 | 00000000 | 0 | |
| **58** | Vertical Border | 00 | 00000000 | 0 | |
| **59** | Bit Encode Sync Information | 18 | 00011000 | 24 | |

| | | | | | |
|---|---|---|---|---|---|
| 5A | DC | 00 | 00000000 | 0 | |
| 5B | HTOTAL | 00 | 00000000 | 0 | |
| 5C | HA | 00 | 00000000 | 0 | |
| 5D | HBL | 00 | 00000000 | 0 | |
| 5E | HFP | 00 | 00000000 | 0 | |
| 5F | HFPe | 00 | 00000000 | 0 | |
| 60 | HBP | 00 | 00000000 | 0 | |
| 61 | HB | 00 | 00000000 | 0 | |
| 62 | HSO | 00 | 00000000 | 0 | nVDPS |
| 63 | HS | 00 | 00000000 | 0 | Reserved 00 |
| 64 | VTOTAL | 00 | 00000000 | 0 | |
| 65 | VA | 00 | 00000000 | 0 | |
| 66 | VBL | 00 | 00000000 | 0 | |
| 67 | VFP | 00 | 00000000 | 0 | |
| 68 | VBP | 00 | 00000000 | 0 | |
| 69 | VB | 00 | 00000000 | 0 | |
| 6A | VSO | 00 | 00000000 | 0 | |
| 6B | VS | 00 | 00000000 | 0 | |
| 6C | Detail Timing Description #4 | 00 | 00000000 | 0 | |
| 6D | Flag | 00 | 00000000 | 0 | |
| 6E | Reserved | 00 | 00000000 | 0 | |
| 6F | For Brightness Table and Power Consumption | 02 | 00000010 | 2 | |
| 70 | Flag | 00 | 00000000 | 0 | Header |
| 71 | PWM % [7:0] @ Step 0 | 10 | 00010000 | 16 | |
| 72 | PWM % [7:0] @ Step 5 | 48 | 01001000 | 72 | |
| 73 | PWM % [7:0] @ Step 10 | FF | 11111111 | 255 | |
| 74 | Nits [7:0] @ Step 0 | 0F | 00001111 | 15 | |
| 75 | Nits [7:0] @ Step 5 | 3C | 00111100 | 60 | |
| 76 | Nits [7:0] @ Step 10 | 6E | 01101110 | 110 | Brightness Table |
| 77 | Panel Electronics Power @ 32x32 Chess Pattern = | 0F | 00001111 | 15 | |
| 78 | Backlight Power @ 60 nits = | 0D | 00001101 | 13 | |
| 79 | Backlight Power @ Step 10 = | 17 | 00010111 | 23 | |
| 7A | Nits @ 100% PWM Duty = | 6E | 01101110 | 110 | Power Consumption |
| 7B | Flag | 20 | 00100000 | 32 | |
| 7C | Flag | 20 | 00100000 | 32 | |
| 7D | Flag | 20 | 00100000 | 32 | |
| 7E | Extension Flag | 00 | 00000000 | 0 | |
| 7F | Checksum | D0 | 11010000 | 208 | |
| | | | SUM | 6400 | |
| | | | SUM to HEX | 1900 | |