

# Model Name: P420IVN03.1

Issue Date : 2022/01/24

(\*) Preliminary Specifications  
( ) Final Specifications

Customer Signature	Date	AUO	Date
Approved By  		Approval By PM Director CT WU  	
Note  		Reviewed By RD Director Lamy Chem  	
		Reviewed By Project Leader Dalon Tseng  	
		Prepared By PM Travis Huang  	

## Contents

Contents.....	2
Record of Revision .....	3
1. General Description .....	4
1.2. Optical Specification.....	5
1.3 Mechanical Characteristics .....	8
3.1 Placement suggestions: .....	8
2. Absolute Maximum Ratings .....	11
3. Electrical Specification .....	12
3.1.1 Electrical Characteristics .....	12
3.1.2 AC Characteristics .....	12
3.3 Input Data Format.....	19
3.4 Signal Timing Specification .....	21
3.5 Signal Timing Waveforms .....	22
3.6 Color Input Data Reference .....	23
3.7 Power Sequence.....	24
Power Sequence of LCD.....	24
Power Sequence of backlight (LED).....	25
3.8 Backlight Specification.....	26
3.7.1 Electrical specification .....	26
3.8.2 Input Pin Assignment .....	27
4. Reliability Test Items .....	29
5. International Standard .....	30
5.1 Safety .....	30
5.2 EMC .....	30
6. Packing .....	31
6-1 DEFINITION OF LABEL: .....	31
6-2 PACKING METHODS: .....	32
7. PRECAUTIONS .....	34
7-1 MOUNTING PRECAUTIONS .....	34
7-2 OPERATING PRECAUTIONS .....	34
7.3 Operating Condition for Public Information Display .....	35
7.4 Electrostatic Discharge Control .....	35
7.5 Precautions for Strong Light Exposure .....	36
7.6 Storage .....	36
7.7 Handling Precautions for Protection Film .....	36
7.8 Dust Resistance .....	36

[illegible]

## 1. General Description

This specification applies to the 42.0 inch Color TFT-LCD Module P420IVN03.1. This LCD module has a TFT active matrix type liquid crystal panel 1,920x480 pixels, and diagonal size of 42.8 inch. This module supports 1,920x480 resolution display. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.

The P420IVN03.1 has been designed to apply the 10-bit 2 channel LVDS interface method. The main feature of P420IVN03.1 would be high brightness, high contrast, wide viewing angle, high color saturation, symmetry narrow bezel, edge LED backlight and high color depth. High Tni (110°C) liquid crystal also applies on this model.

### \* General Information

Items	Specification	Unit	Note
Active Screen Size	42.8	Inch	
Display Area	1039.68(H) x 259.92(V)	mm	
Outline Dimension	1059.48(H) x 283.32(V) x 27.2(D)	mm	1
Driver Element	a-Si TFT active matrix		
Display Colors	10 bit (8bit+FRC), 1073.7M	Colors	
Number of Pixels	1,920x480	Pixel	
Pixel Pitch	0.54 (H) x 0.54(W)	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Display Orientation	Landscape/Portrait Enable		
Surface Treatment	AG,3H		Haze = 28%

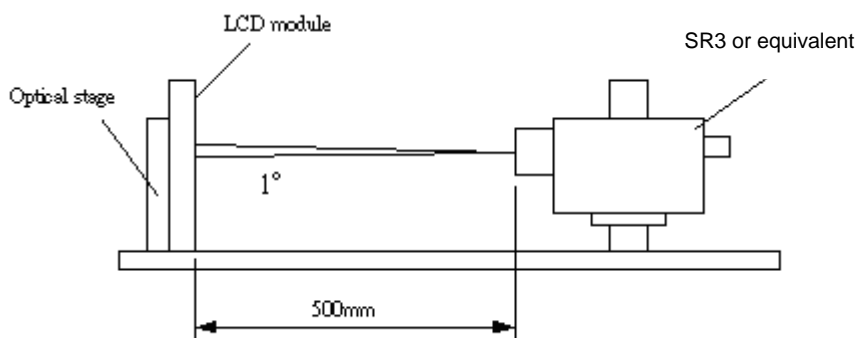
Note:

- (1) D<sub>max</sub>:56.9mm (Front bezel to Driver cover); D<sub>min</sub>: 27.2mm (Front bezel to Bezel back)

## 1.2. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25°C while panel is placed in the default position. The default position is T-con side as the top side of panel. The value specified is at an approximate distance 50cm from the LCD surface at a viewing angle of  $\varphi$  and  $\theta$  equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter		Symbol	Values			Unit	Notes
			Min.	Typ.	Max		
Contrast Ratio		CR	3200	4000	--		1
Surface Luminance (White)		L <sub>WH</sub>	2000	2500	--	cd/m <sup>2</sup>	2
Luminance Variation		$\delta_{\text{WHITE(9P)}}$	--	--	1.33		3
Response Time (G to G)		T <sub>γ</sub>	--	8	--	ms	4
Color Gamut		sRGB		72		%	
Color Coordinates							
	Red	R <sub>x</sub>	Typ.-0.03	0.604(TBD)	Typ.+0.03		
		R <sub>y</sub>		0.320(TBD)			
	Green	G <sub>x</sub>		0.321(TBD)			
		G <sub>y</sub>		0.573(TBD)			
	Blue	B <sub>x</sub>		0.161(TBD)			
		B <sub>y</sub>		0.100(TBD)			
	White	W <sub>x</sub>		0.290(TBD)			
		W <sub>y</sub>		0.300(TBD)			
Viewing Angle							5
	x axis, right( $\varphi=0^\circ$ )	$\theta_r$	--	89	--	degree	
	x axis, left( $\varphi=180^\circ$ )	$\theta_l$	--	89	--	degree	
	y axis, up( $\varphi=90^\circ$ )	$\theta_u$	--	89	--	degree	
	y axis, down ( $\varphi=270^\circ$ )	$\theta_d$	--	89	--	degree	

Note:

1. Contrast Ratio (CR) is defined mathematically as:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance of } L_{on5}}{\text{Surface Luminance of } L_{off5}}$$

2. Surface luminance is luminance value at point 5 across the LCD surface 50cm from the surface with all pixels displaying white. From more information see FIG 2. When lamp current  $I_H = 11\text{mA}$ .  $L_{WH} = L_{on5}$  where  $L_{on5}$  is the luminance with all pixels displaying white at center 5 location.

3. The variation in surface luminance,  $\delta_{WHITE}$  is defined (center of Screen) as:

$$\delta_{WHITE(9P)} = \frac{\text{Maximum}(L_{on1}, L_{on2}, \dots, L_{on9})}{\text{Minimum}(L_{on1}, L_{on2}, \dots, L_{on9})}$$

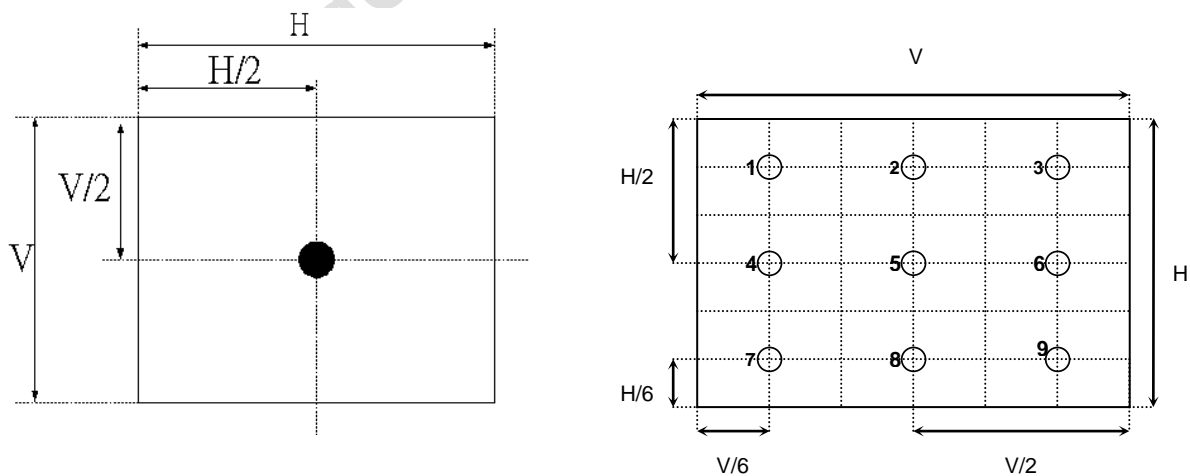
4. Response time  $T_\gamma$  is the average time required for display transition by switching the input signal for five luminance ratio (0%, 25%, 50%, 75%, 100% brightness matrix) and is based on  $F_v = 60\text{Hz}$  to optimize.

$T_\gamma$  is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

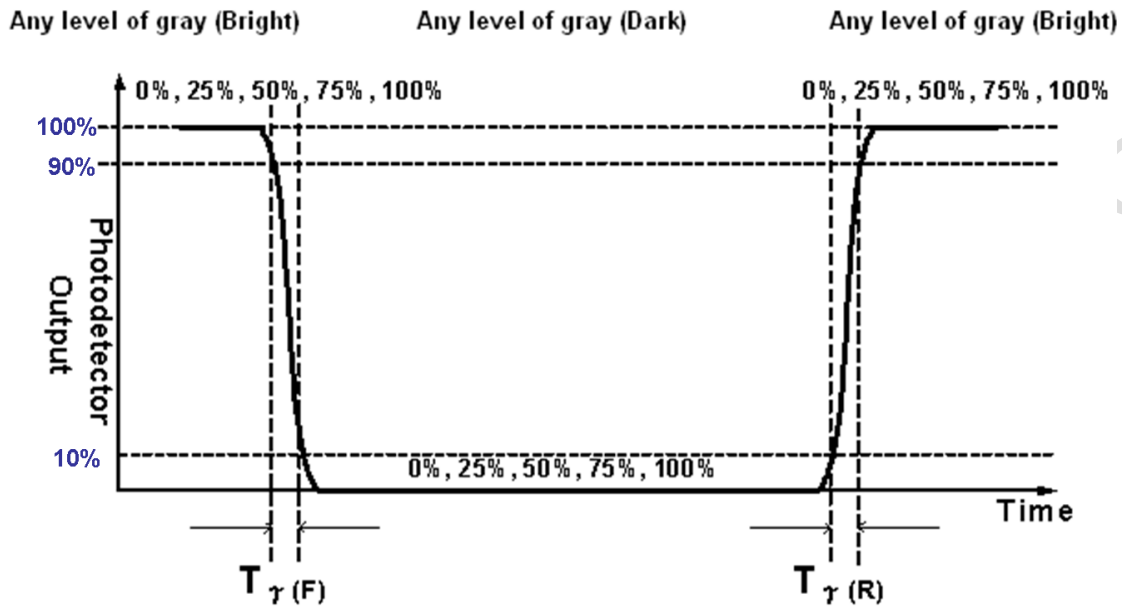
5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG4.

**FIG. 2 Luminance**

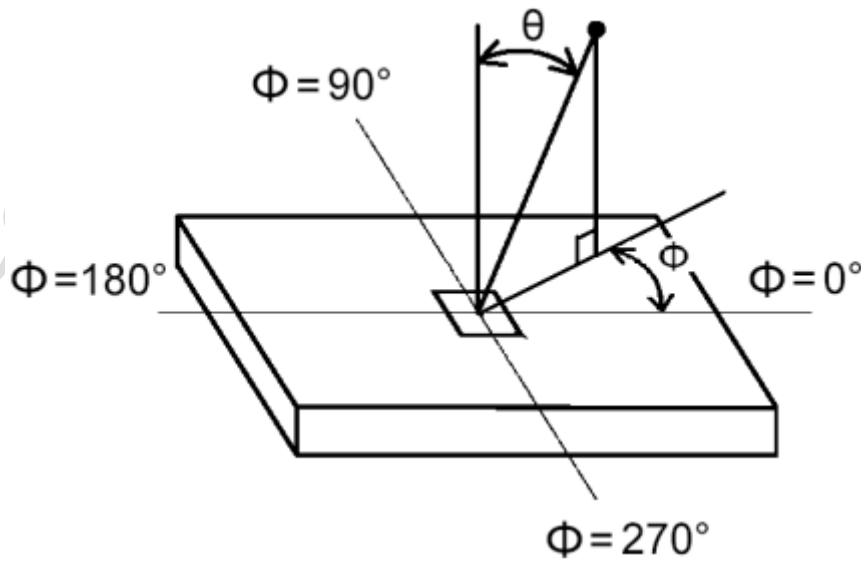


**FIG.3 Response Time**

The response time is defined as the following figure and shall be measured by switching the input signal for “any level of gray(bright)” and “any level of gray(dark)”.



**FIG.4 Viewing Angle**



## 1.3 Mechanical Characteristics

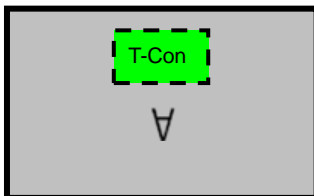
The contents provide general mechanical characteristics for the model P420IVN03.1. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal (typ.)	1059.48mm
	Vertical (typ.)	283.32mm
	Depth (min.)	27.2mm
Bezel Opening Area	Horizontal (typ.)	1043.68 mm
	Vertical (typ.)	263.92 mm
Active Display Area	Horizontal	1039.68 mm
	Vertical	259.92 mm
Weight	5500(g)	

### 3.1 Placement suggestions:

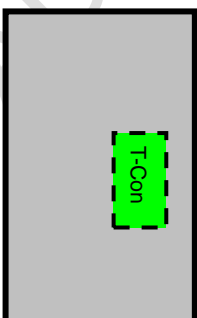
1. Landscape Mode: The default placement is T-Con Side on the lower side and the image is shown upright via viewing from the front.

Landscape (Front view)



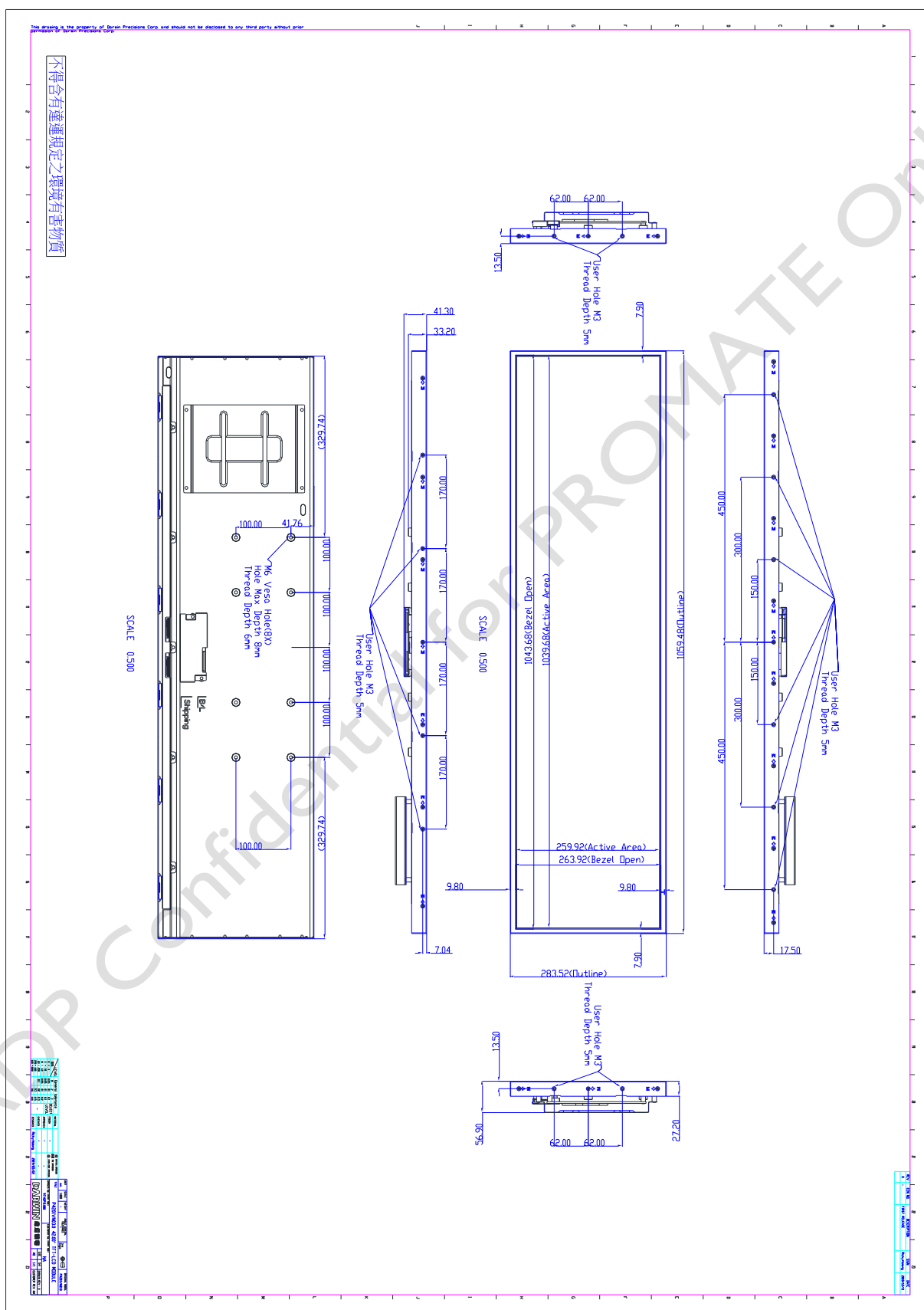
2. Portrait Mode: The default placement is that T-Con side has to be placed on the left side via viewing from the front.

Portrait (Front view)

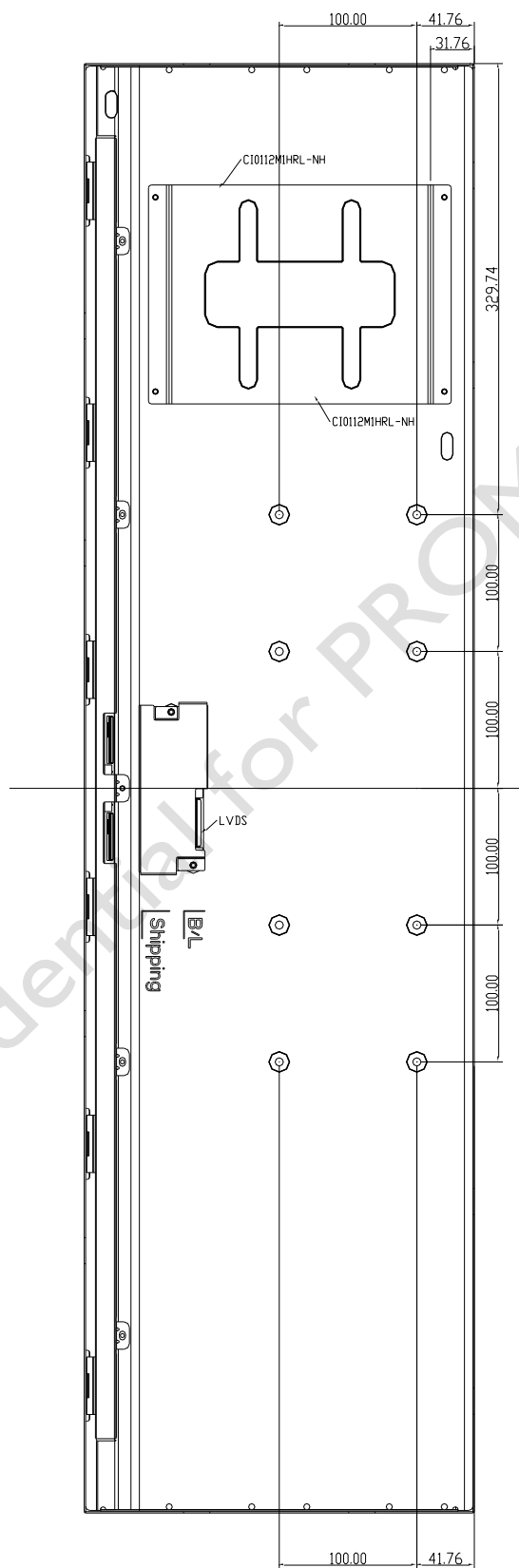




### Front View



## Rear View



## 2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit

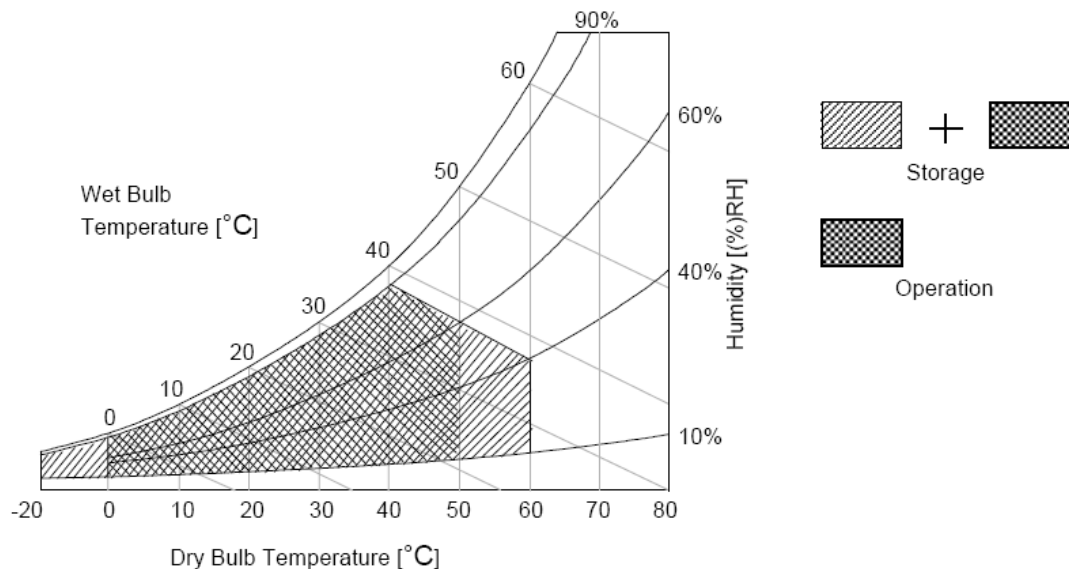
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vcc	-0.3	14	[Volt]	Note 1
Input Voltage of Signal	Vin	-0.3	4	[Volt]	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	Note 3

Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39°C and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40°C or less. At temperatures greater than 40°C, the wet bulb temperature must not exceed 39°C.

Note 3: Surface temperature is measured at 50°C Dry condition



### 3. Electrical Specification

The P420IVN03.1 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second is employed for LED driver.

#### 3.1.1 Electrical Characteristics

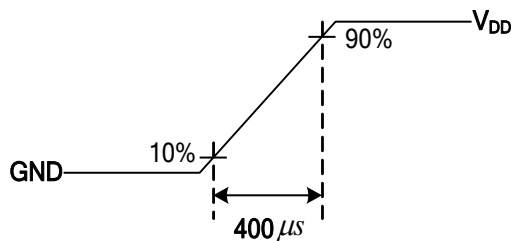
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LCD							
Power Supply Input Voltage		V <sub>DD</sub>	10.8	12	13.2	V <sub>DC</sub>	
Power Supply Input Current		I <sub>DD</sub>	--	0.516	0.619	A	1
Power Consumption		P <sub>C</sub>	--	6.192	7.43	Watt	1
Inrush Current		I <sub>RUSH</sub>	-	-	1.44	A	2
Permissible Ripple of Power Supply Input Voltage (for input power=12V)		V <sub>RP</sub>	--	--	V <sub>DD</sub> * 5%	mV <sub>pk-pk</sub>	3
LVDS Interface	Input Differential Voltage	V <sub>ID</sub>	200	400	600	mV <sub>DC</sub>	4
	Differential Input High Threshold Voltage	V <sub>TH</sub>	+100	--	+300	mV <sub>DC</sub>	4
	Differential Input Low Threshold Voltage	V <sub>TL</sub>	-300	--	-100	mV <sub>DC</sub>	4
	Input Common Mode Voltage	V <sub>ICM</sub>	1.1	1.25	1.4	V <sub>DC</sub>	4
CMOS Interface	Input High Threshold Voltage	V <sub>IH</sub> (High)	2.7	--	3.3	V <sub>DC</sub>	7
	Input Low Threshold Voltage	V <sub>IL</sub> (Low)	0	--	0.6	V <sub>DC</sub>	
Backlight Power Consumption		P <sub>BL</sub>	--	96(TBD)		W	
LED MTTF		LED_MTTF	50000			--	8

#### 3.1.2 AC Characteristics

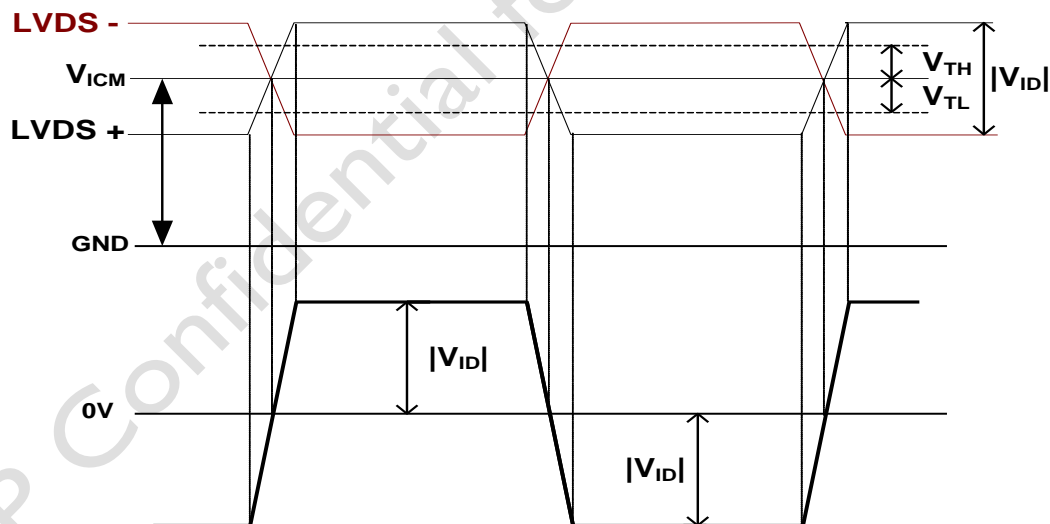
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	9
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	--	200	KHz	9
	Receiver Data Input Margin Fclk = 85 MHz Fclk = 65 MHz	tRMG	-0.4 -0.5	-- --	0.4 0.5	ns	10

**Note :**

1. Test Condition:
  - (1)  $V_{DD} = 12.0V$
  - (2)  $F_v =$  Type Timing, 60Hz, 120Hz or Other
  - (3)  $F_{CLK} =$  Max freq.
  - (4) Temperature = 25 °C
  - (5) Test Pattern : White Pattern
2. Measurement condition : Rising time = 400us



3. Test Condition:
  - (1) The measure point of  $V_{RP}$  is in LCM side after connecting the System Board and LCM.
  - (2) Under Max. Input current spec. condition.
4.  $V_{ICM} = 1.25V$



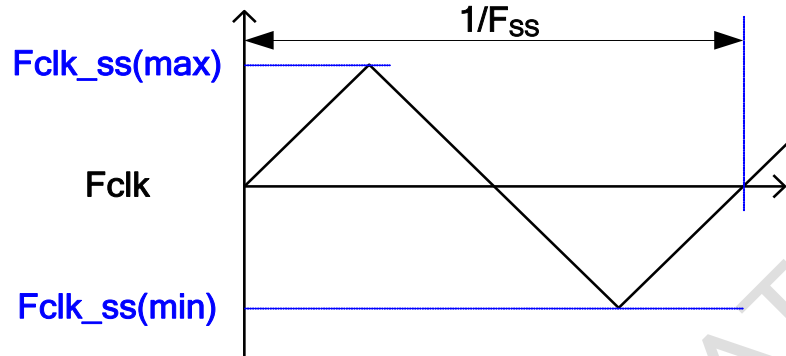
5. Do not attach a conducting tape to lamp connecting wire. If the lamp wire attach to conducting tape, TFT-LCD Module have a low luminance and the inverter has abnormal action because leakage current occurs between lamp wire and conducting tape.
6. The relative humidity must not exceed 80% non-condensing at temperatures of 40°C or less. At temperatures greater than 40°C, the wet bulb temperature must not exceed 39°C. When operate at high temperatures, the brightness of LED will drop and the life time of LED will be reduced.
7. The measure points of  $V_{IH}$  and  $V_{IL}$  are in LCM side after connecting the System Board and LCM.

8. LED MTTF is defined as the time which luminance of LED is 50% compared to its original value.

[Operating condition: Continuous operating at  $T_a = 25 \pm 2^\circ\text{C}$ , for single LED only]

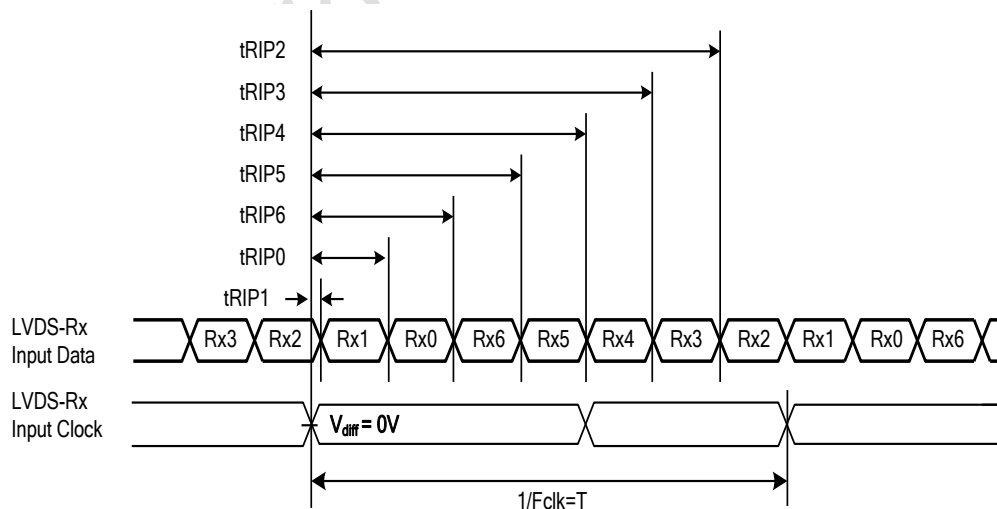
MTTF is a reference index, it is not representative of warranty.

9. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures



10. Receiver Data Input Margin

Parameter	Symbol	Rating			Unit	Note
		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	$T=1/F_{clk}$
Input Data Position0	tRIP1	- tRMG	0	tRMG	ns	
Input Data Position1	tRIP0	$T/7 -  tRMG $	$T/7$	$T/7 +  tRMG $	ns	
Input Data Position2	tRIP6	$2T/7 -  tRMG $	$2T/7$	$2T/7 +  tRMG $	ns	
Input Data Position3	tRIP5	$3T/7 -  tRMG $	$3T/7$	$3T/7 +  tRMG $	ns	
Input Data Position4	tRIP4	$4T/7 -  tRMG $	$4T/7$	$4T/7 +  tRMG $	ns	
Input Data Position5	tRIP3	$5T/7 -  tRMG $	$5T/7$	$5T/7 +  tRMG $	ns	
Input Data Position6	tRIP2	$6T/7 -  tRMG $	$6T/7$	$6T/7 +  tRMG $	ns	

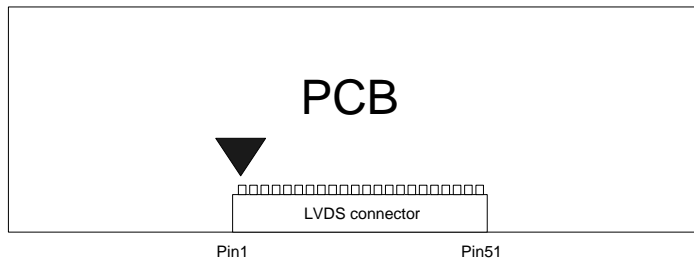


### 3.2 Interface Connections

**LCD connector :** LCD connector: JAE FI-RTE51SZ-HF

PIN	Symbol	Description	Note	PIN	Symbol	Description	Note
1	N.C.	No connection	2	26	N.C.	No connection	2
2	N.C.	No connection (for AUO internal only)	3&5	27	N.C.	No connection	2
3	N.C.	No connection (for AUO internal only)	3&7	28	CH2_0-	LVDS Channel 2, Signal 0-	
4	N.C.	No connection (for AUO internal only)	3&5	29	CH2_0+	LVDS Channel 2, Signal 0+	
5	BITSEL	LVDS 8/10bit input selection Open/ Low (GND): 8bits High (3.3V): 10bit	3&6	30	CH2_1-	LVDS Channel 2, Signal 1-	
6	N.C.	No connection	2	31	CH2_1+	LVDS Channel 2, Signal 1+	
7	LVDS_SEL	Open/ High (3.3V) for NS Low (GND) for JEIDA	3&4	32	CH2_2-	LVDS Channel 2, Signal 2-	
8	N.C.	No connection	2	33	CH2_2+	LVDS Channel 2, Signal 2+	
9	N.C.	No connection	2	34	GND	Ground	
10	N.C.	No connection	2	35	CH2_CLK-	LVDS Channel 2, Clock -	
11	GND	Ground		36	CH2_CLK+	LVDS Channel 2, Clock +	
12	CH1_0-	LVDS Channel 1, Signal 0-		37	GND	Ground	
13	CH1_0+	LVDS Channel 1, Signal 0+		38	CH2_3-	LVDS Channel 2, Signal 3-	
14	CH1_1-	LVDS Channel 1, Signal 1-		39	CH2_3+	LVDS Channel 2, Signal 3+	
15	CH1_1+	LVDS Channel 1, Signal 1+		40	CH2_4-	LVDS Channel 2, Signal 4-	
16	CH1_2-	LVDS Channel 1, Signal 2-		41	CH2_4+	LVDS Channel 2, Signal 4+	
17	CH1_2+	LVDS Channel 1, Signal 2+		42	N.C.	No connection	2
18	GND	Ground		43	N.C.	No connection	2
19	CH1_CLK-	LVDS Channel 1, Clock -		44	GND	Ground	
20	CH1_CLK+	LVDS Channel 1, Clock +		45	GND	Ground	
21	GND	Ground		46	GND	Ground	
22	CH1_3-	LVDS Channel 1, Signal 3-		47	N.C.	No connection	2
23	CH1_3+	LVDS Channel 1, Signal 3+		48	V <sub>DD</sub>	Power Supply Input Voltage	
24	CH1_4-	LVDS Channel 1, Signal 4-		49	V <sub>DD</sub>	Power Supply Input Voltage	
25	CH1_4+	LVDS Channel 1, Signal 4+		50	V <sub>DD</sub>	Power Supply Input Voltage	
				51	V <sub>DD</sub>	Power Supply Input Voltage	

Note1. Pin number start from the left side as the following figure.



Note2. Please leave this pin unoccupied. It can not be connected by any signal (Low/GND/High).

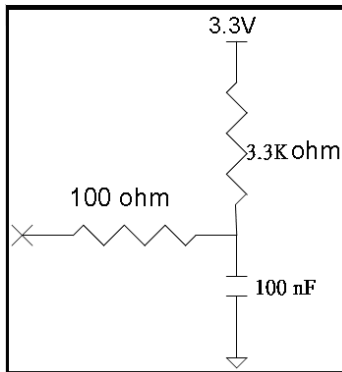
Note3. Input control signal threshold voltage definition

Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	VIH	2.7	-	3.6	V
Input Low Threshold Voltage	VIL	0	-	0.6	V

Note4. LVDS data format selection

LVDS_SEL	Mode
H or OPEN	NS
L	Jeida

Input equivalent impedance of LVDE\_SEL pin



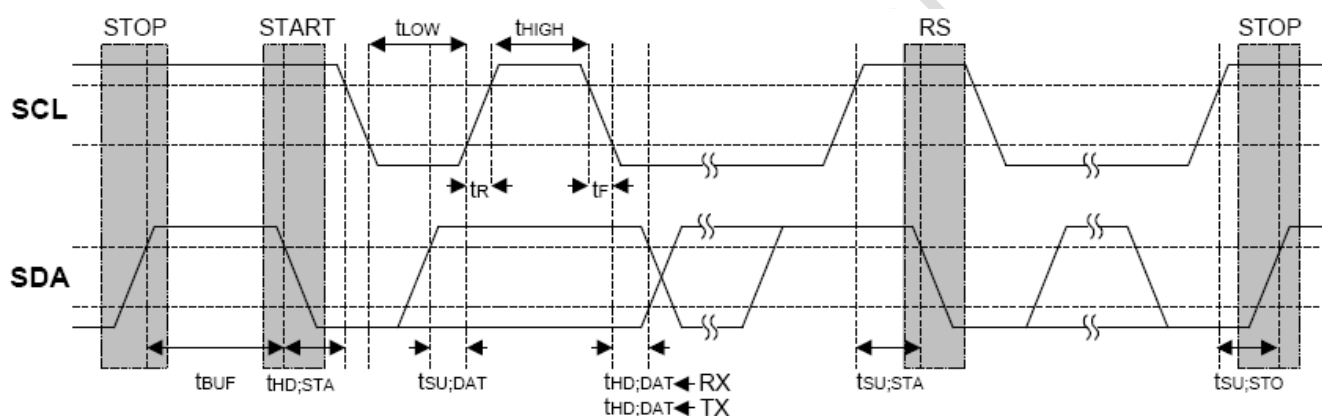
Note5. I2C Data and Clock

I2C Data and Clock timing

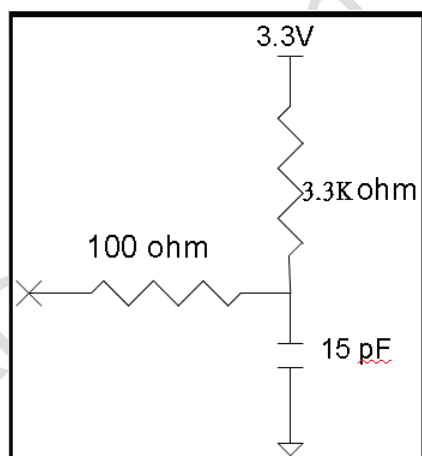
Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max	Min	Max	
fSCL	SCL Clock Frequency		100		400	KHz
tBUF	Bus Free Between a STOP and START Condition	4.7		1.3		us



t <sub>HD;STA</sub>	Hold Time for START Condition	4.0		0.6		us
t <sub>LOW</sub>	LOW Period of The SCL Clock	4.7		1.3		us
t <sub>HIGH</sub>	HIGH Period of The SCL Clock	4.0		0.6		us
t <sub>SU;STA</sub>	Set-up Time for a Repeated START Condition	4.7		0.6		us
t <sub>HD;DAT</sub>	Data Hold Time	Transmitter	0.1		0.1	0.9 us
		Receiver	0		0	
t <sub>SU;DAT</sub>	Data Set-up Time	250		100		ns
T <sub>r</sub>	Rise Time of Both SDA and SCL Signals		1000		300	ns
t <sub>f</sub>	Fall Time of Both SDA and SCL Signals		300		300	ns
t <sub>SU;STO</sub>	Set-up Time for STOP Condition	4.0		0.6		us
t <sub>SP</sub>	Pulse Width of spikes which must be suppressed by the input filter	0	50	0	50	ns
C <sub>I</sub>	Capacitance for each Bus Pin	-	10		10	pF
C <sub>b</sub>	Capacitive load for each Bus Line	-	400		400	pF



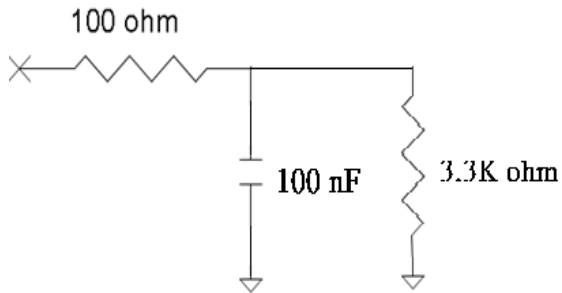
#### Input equivalent impedance of SDA/SCL pin



**Note6. Data Bit mode format selection**

BIT_SEL	Mode
H	10Bit
L or OPEN	8Bit

**Input equivalent impedance of BIT\_SEL pin**

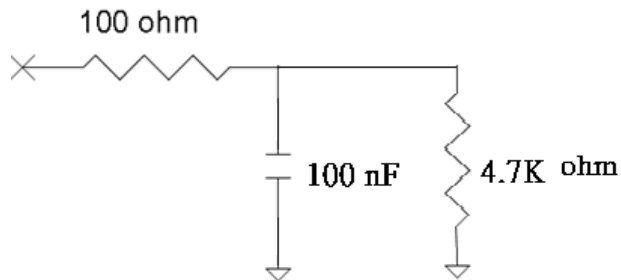


**Note7. Write Protection**

**Mode selection**

WP	Note
L or OPEN	Protection
H	Writable

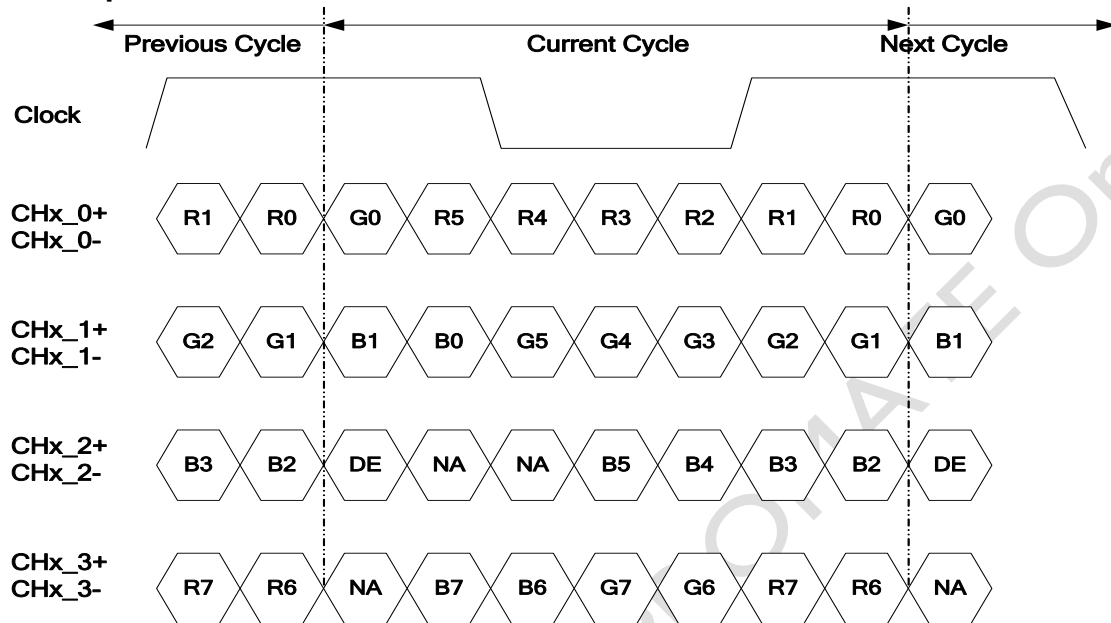
**Input equivalent impedance of WP pin**



### 3.3 Input Data Format

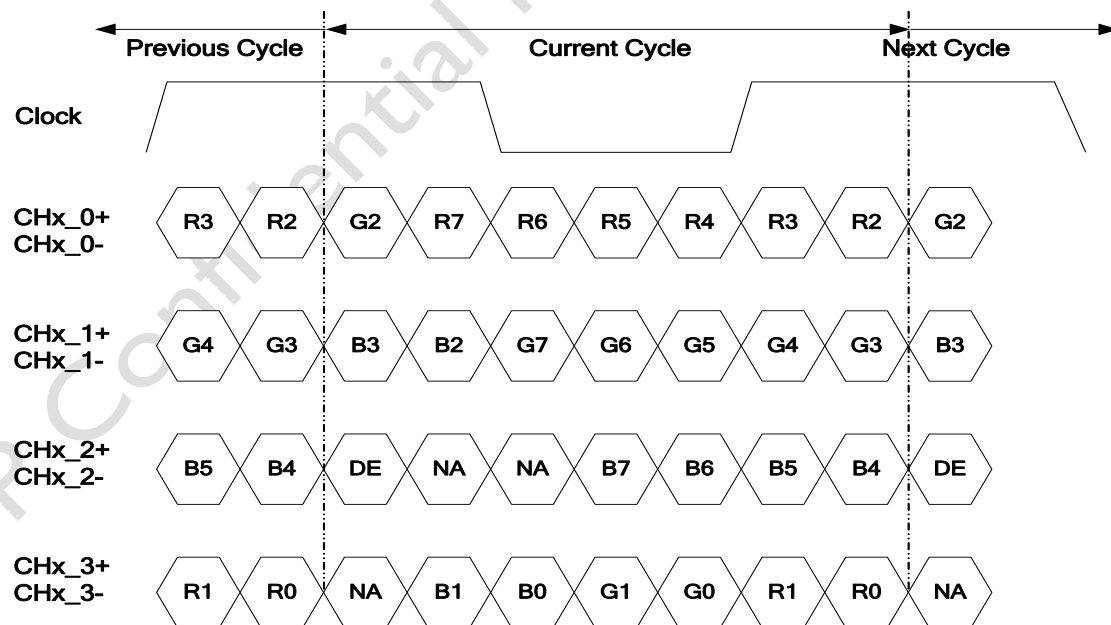
#### LVDS Option for 8bit

##### ■ LVDS Option NS



Note: x = 1, 2, 3, 4...

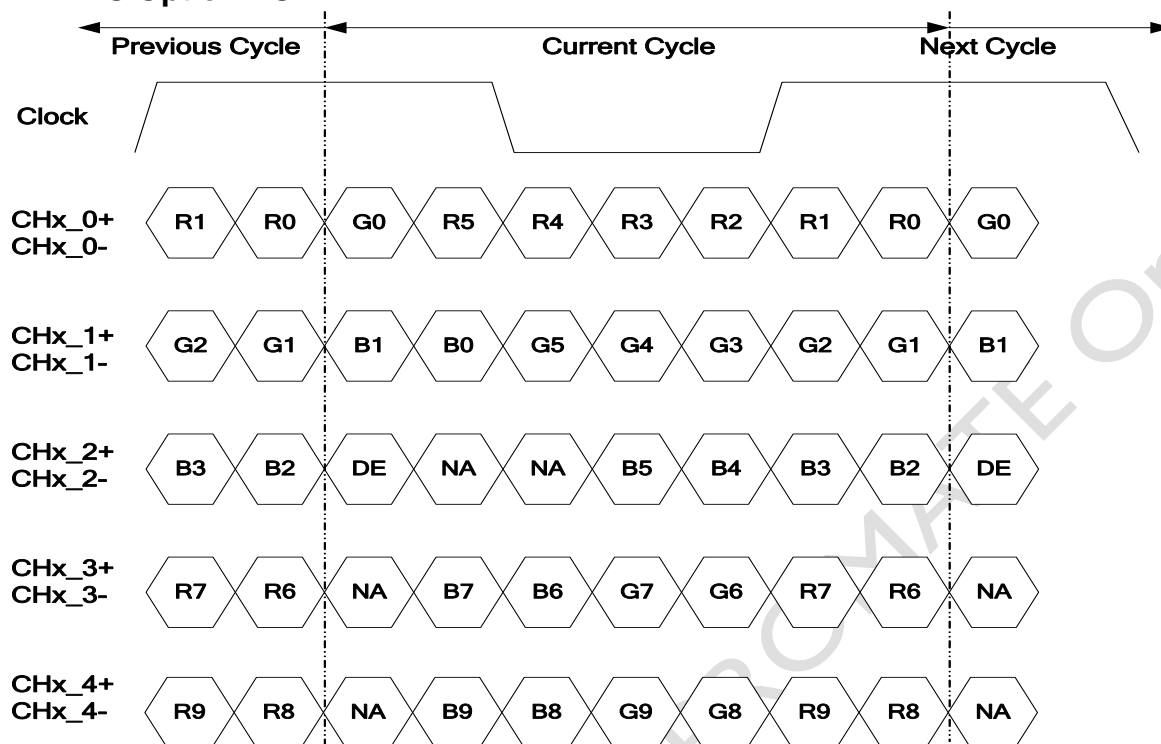
##### ■ LVDS Option JEIDA



Note: x = 1, 2, 3, 4...

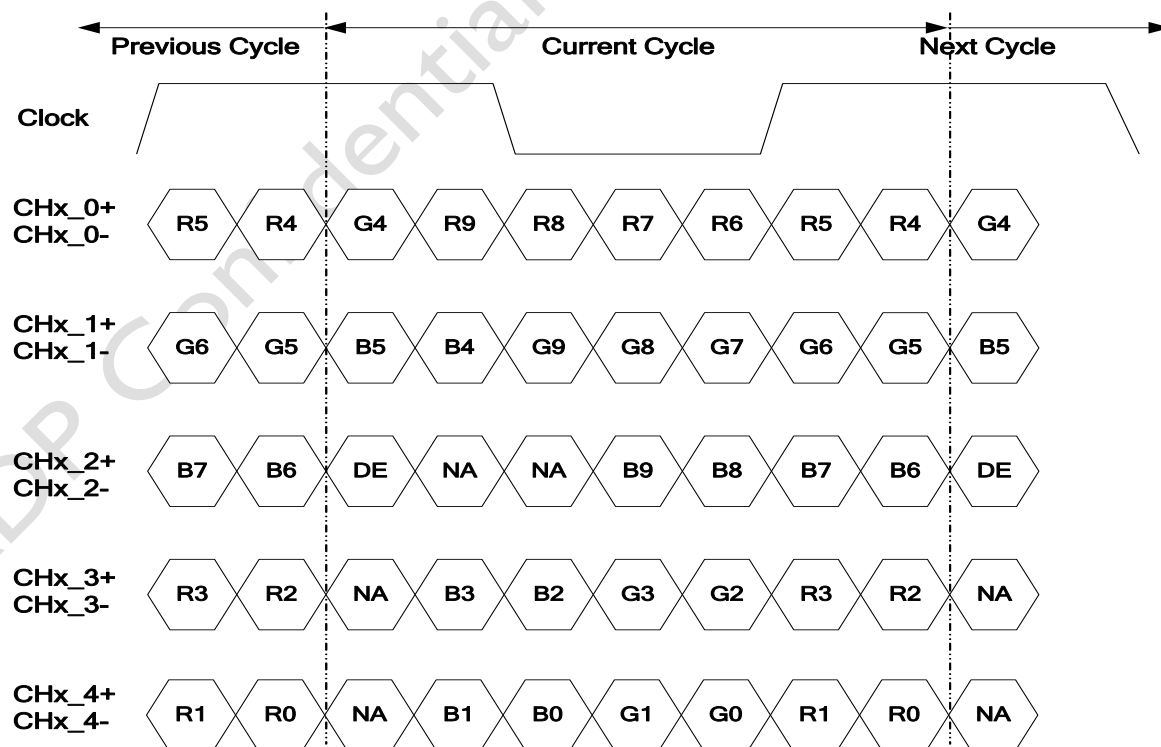
## LVDS Option for 10bit

### ■ LVDS Option NS



Note: x = 1, 2, 3, 4...

### ■ LVDS Option JEIDA



Note: x = 1, 2, 3, 4...

### 3.4 Signal Timing Specification

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

#### Timing Table (DE only Mode)

##### Vertical Frequency Range (60Hz)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	500	585	860	Th
	Active	Tdisp (v)	480			
	Blanking	Tblk (v)	20	105	380	Th
Horizontal Section	Period	Th	1200	1282	1325	Tclk
	Active	Tdisp (h)	960			
	Blanking	Tblk (h)	240	322	365	Tclk
Clock	Frequency	Fclk=1/Tclk	42	45	48	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	33.6	35.1	36.6	KHz

Notes:

(1) Display position is specific by the rise of DE signal only.

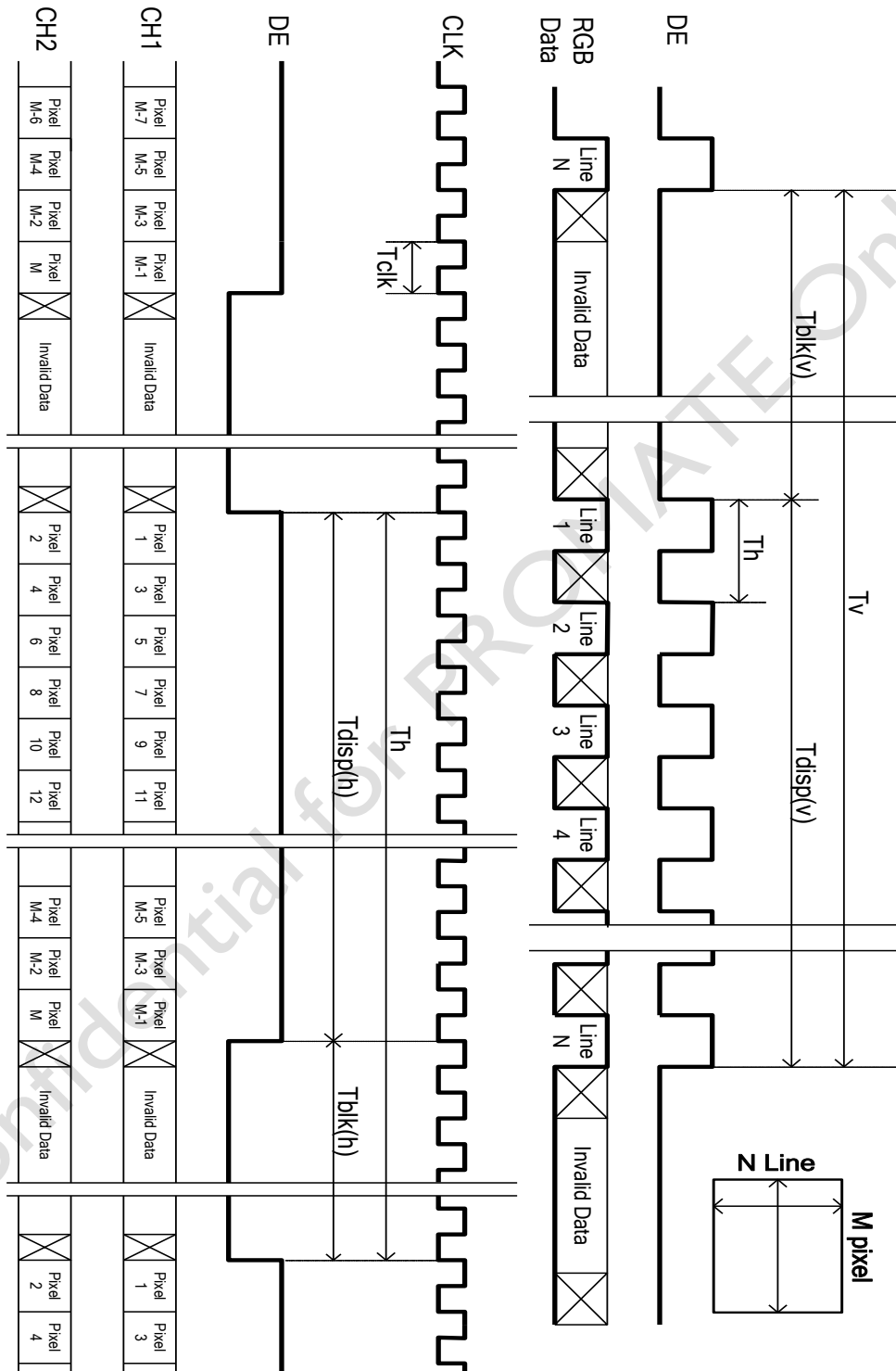
Horizontal display position is specified by the rising edge of 1<sup>st</sup> DCLK after the rise of 1<sup>st</sup> DE, is displayed on the left edge of the screen.

(2) Vertical display position is specified by the rise of DE after a "Low" level period equivalent to eight times of horizontal period. The 1<sup>st</sup> data corresponding to one horizontal line after the rise of 1<sup>st</sup> DE is displayed at the top line of screen.

(3) If a period of DE "High" is less than 1920 DCLK or less than 480 lines, the rest of the screen displays black.

(4) The display position does not fit to the screen if a period of DE "High" and the effective data period do not synchronize with each other.

### 3.5 Signal Timing Waveforms



### 3.6 Color Input Data Reference

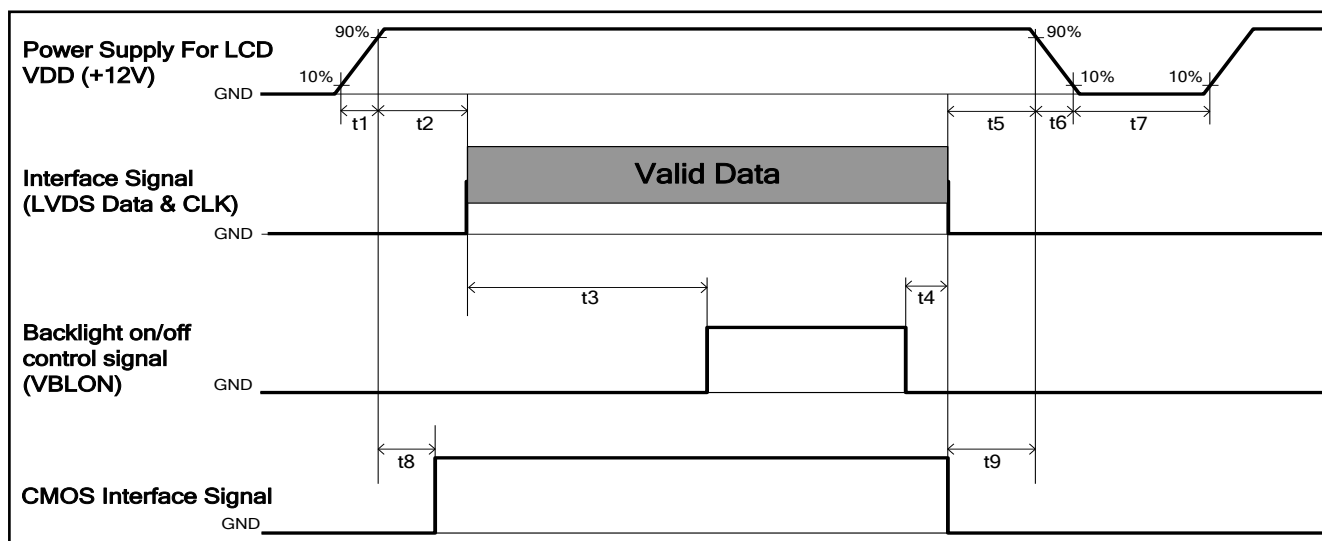
The brightness of each primary color (red, green and blue) is based on the 10 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

Color		Input Color Data																															
		RED										GREEN										BLUE											
		MSB					LSB					MSB					LSB					MSB						LSB					
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0		
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0		
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1		
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1		
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0		
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	----																																
	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0		
	----																																
	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0		
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0		
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1		
	----																																
	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0		
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1		

### 3.7 Power Sequence

#### ◆ Power Sequence of LCD



Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	0.1	---	50	ms
t3	450	---	---	ms
t4	0 <sup>*1</sup>	---	---	ms
t5	0	---	---	ms
t6	---	---	--- <sup>*2</sup>	ms
t7	500	---	---	ms
t8	10	---	50	ms
t9	0	---	---	ms

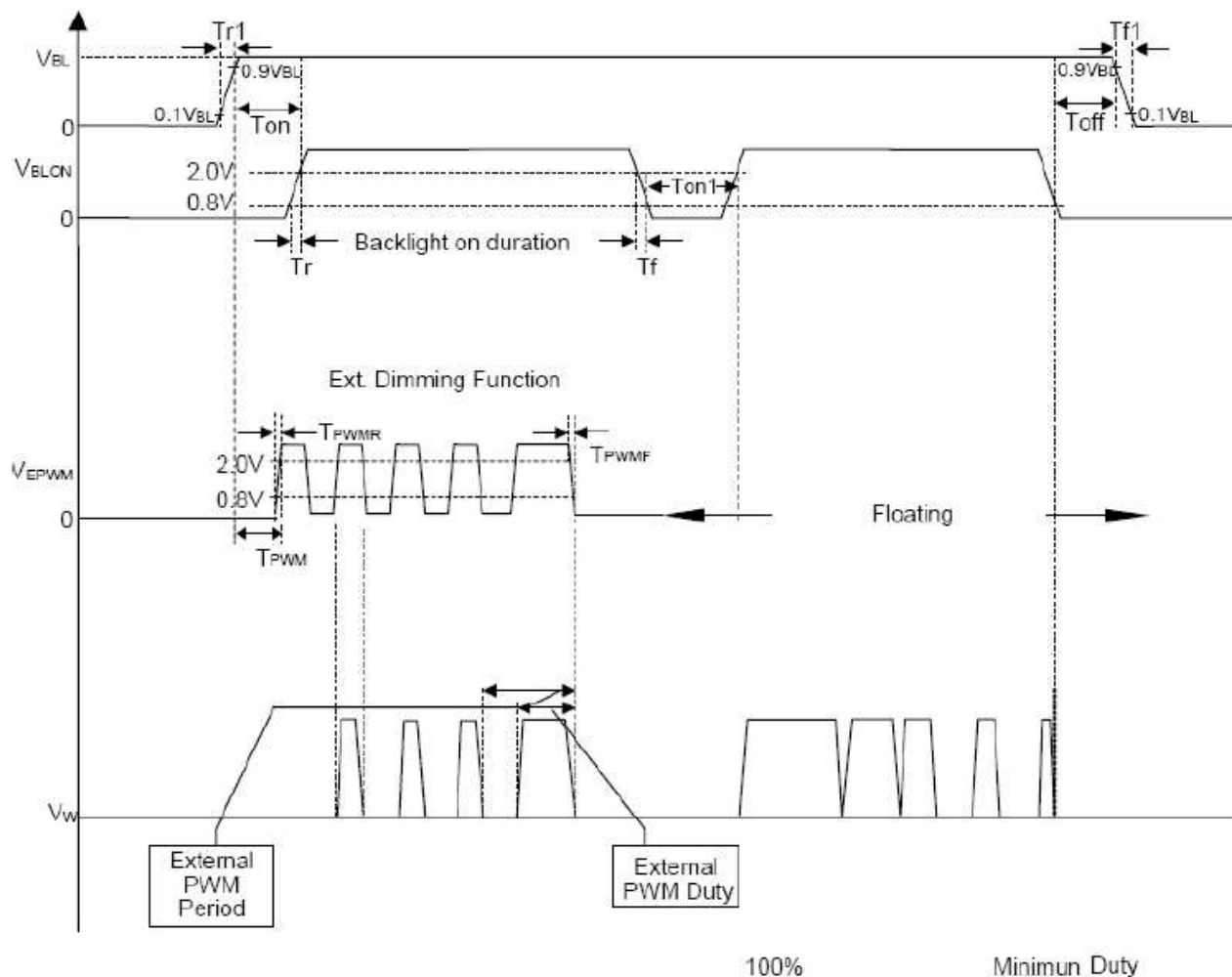
Note:

(1) t4=0 : concern for residual pattern before BLU turn off.

(2) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)



◆ **Power Sequence of backlight (LED)**



**Fig.1**

ITEM	SYMBOL	CONDITION TEST	MIN	TYPE	MAX	UNIT	
Control Signal Rising Time	Tr	—	—	—	100	ms	See Fig.1
Control Signal Falling Time	Tf	—	—	—	100	ms	
VBL Rising Time	Tr1	—	30	—	—	ms	
VBL Falling Time	Tf1	—	30	—	—	ms	
PWM Signal Rising Time	TPWMR	—	—	—	50	us	
PWM Signal Falling Time	TPWMF	—	—	—	50	us	

### 3.8 Backlight Specification

The backlight unit contains 80pcs LED.

#### 3.7.1 Electrical specification

	Item	Symbol	Condition	Spec			Unit	Note
				Min	Typ	Max		
1	Input Voltage	V <sub>DDB</sub>	-	21.6	24	26.4	VDC	-
2	Input Current	I <sub>DDB</sub>	V <sub>DDB</sub> =24V	--	4.0 (TBD)		ADC	1
3	Input Power	P <sub>DDB</sub>	V <sub>DDB</sub> =24V	--	96 (TBD)		W	1
4	Inrush Current	I <sub>RUSH</sub>	V <sub>DDB</sub> =24V	-	-	TBD	ADC	2
5	On/Off control voltage	V <sub>B<sub>LON</sub></sub>	V <sub>DDB</sub> =24V	2	-	5.5	VDC	-
				0	-	0.8		-
6	On/Off control current	I <sub>B<sub>LON</sub></sub>	V <sub>DDB</sub> =24V	-	-	1.5	mA	-
7	External PWM Control Voltage	V <sub>EPWM</sub>	MAX	V <sub>DDB</sub> =24V	2	-	VDC	-
			MIN	V <sub>DDB</sub> =24V	0	-		-
8	External PWM Control Current	I <sub>EPWM</sub>	V <sub>DDB</sub> =24V	-	-	2	mADC	-
9	External PWM Duty ratio	D <sub>EPWM</sub>	V <sub>DDB</sub> =24V	20	-	100	%	3
10	External PWM Frequency	F <sub>EPWM</sub>	V <sub>DDB</sub> =24V	6000	6500	7000	Hz	-
11	DET status signal	DET	V <sub>DDB</sub> =24V	Open Collector			VDC	-
				0	-	0.8	VDC	-
12	Input Impedance	R <sub>in</sub>	V <sub>DDB</sub> =24V	300			Kohm	-

Note 1 : Dimming ratio= 100% (MAX) ( Ta=25±5°C, Turn on for 45minutes )

Note 2: Measurement condition Rising time = 20ms (V<sub>DDB</sub> : 20%~90%) and at dimming ratio = 100%

Note 3: Less than 20% dimming control is functional well and no backlight shutdown happened

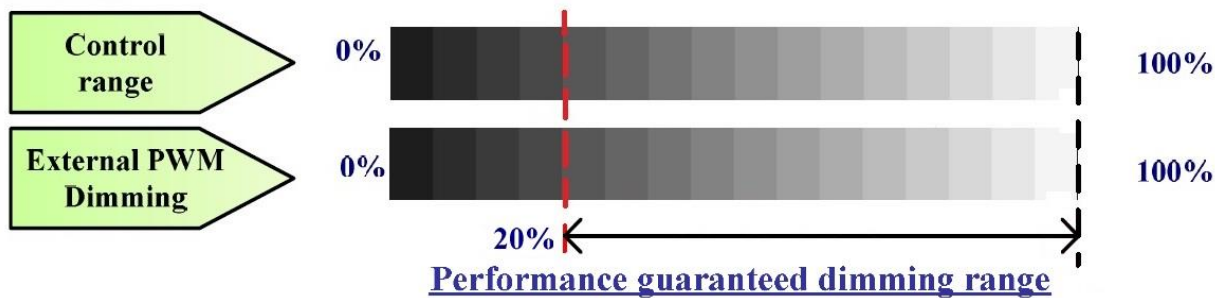
### 3.8.2 Input Pin Assignment

LED driver board connector: CI0114M1HRL-NH(CviLux)

Pin	Symbol	Description
1	VDDDB	Operating Voltage Supply, +24V DC regulated
2	VDDDB	Operating Voltage Supply, +24V DC regulated
3	VDDDB	Operating Voltage Supply, +24V DC regulated
4	VDDDB	Operating Voltage Supply, +24V DC regulated
5	VDDDB	Operating Voltage Supply, +24V DC regulated
6	BLGND	Ground and Current Return
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	DET	BLU status detection: Normal : GND ; Abnormal : Open collector
12	VBLON	BLU On-Off control: BL On : High/Open (2V~5.5V); BL off : GND
13	NC	NC
14	PDIM	External PWM (20%~100% Duty, open for 100%)

LED driver board connector: CI0112M1HRL-NH(CviLux)

Pin	Symbol	Description
1	VDDDB	Operating Voltage Supply, +24V DC regulated
2	VDDDB	Operating Voltage Supply, +24V DC regulated
3	VDDDB	Operating Voltage Supply, +24V DC regulated
4	VDDDB	Operating Voltage Supply, +24V DC regulated
5	VDDDB	Operating Voltage Supply, +24V DC regulated
6	BLGND	Ground and Current Return
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	NC	No connection
12	NC	No connection



(Note\*) IF External PWM function includes 20% dimming ratio. Judge condition as below:

- (1) Backlight module must be lighted ON normally.
- (2) All protection function must work normally.
- (3) Uniformity and flicker could NOT be guaranteed

## 4. Reliability Test Items

	Test Item	Q'ty	Condition
1	High temperature storage test	3	60°C, 500hrs
2	Low temperature storage test	3	-20°C, 500hrs
3	High temperature operation test	3	50°C, 500hrs
4	Low temperature operation test	3	-10°C, 500hrs
5	Vibration test (With carton)	1 (PKG)	Random wave (1.04G RMS, 2-200Hz) 20 mins per each X,Y,Z axes PSD( $G^2/Hz$ ) at different frequency show as below 2Hz, 0.0010 4Hz, 0.0300 8Hz, 0.0300 40Hz, 0.0030 55Hz, 0.0100 75Hz, 0.0100 200Hz, 0.0008
6	Drop test (With carton)	1 (PKG)	Drop Height: 25.4cm, Surround four flats and bottom flat twice (ASTMD4169)

## 5. International Standard

### 5.1 Safety

- (1) UL 62368-1 : Audio/video, information and communication technology equipment – Part 1: Safety requirements
- (2) IEC 62368-1 : Audio/video, information and communication technology equipment –Part 1: Safety requirements
- (3) EN 62368-1 : Audio/video, information and communication technology equipment –Part 1: Safety requirements

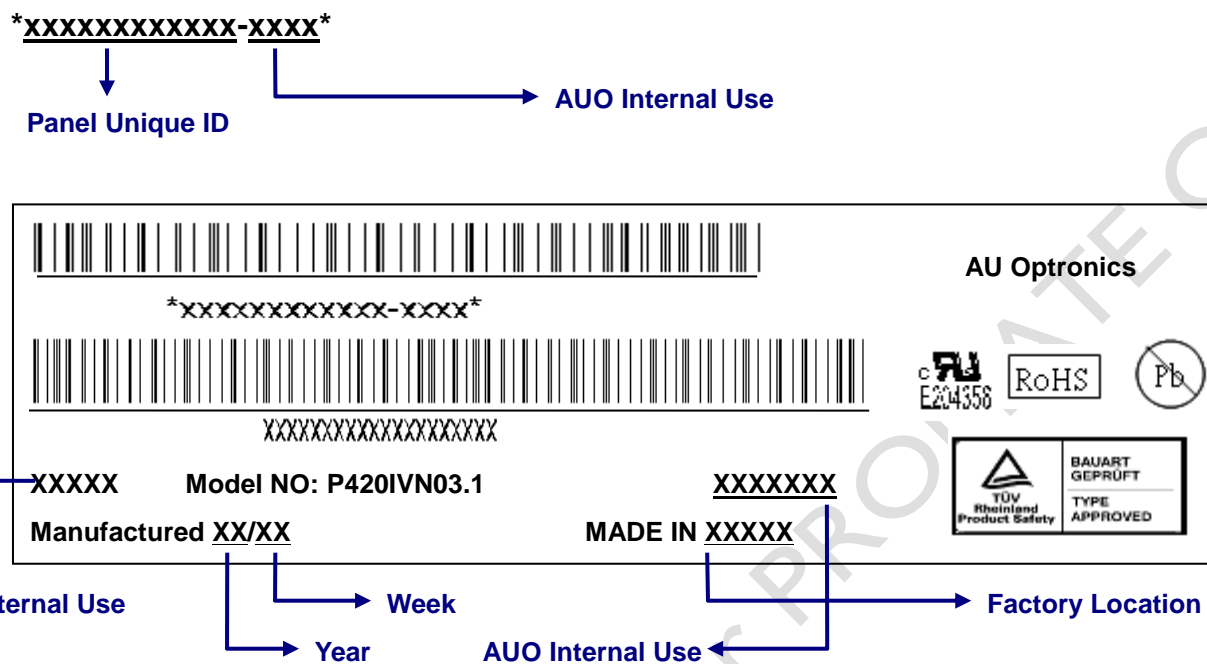
### 5.2 EMC

- (1) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. “American National standards Institute(ANSI), 1992
- (2) C.I.S.P.R “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” International Special committee on Radio Interference.
- (3) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” European Committee for Electro technical Standardization. (CENELEC), 1998

## 6. Packing

### 6-1 DEFINITION OF LABEL:

#### A. Panel Label:



#### Green mark description

(1) For Pb Free Product, AUO will add for identification.

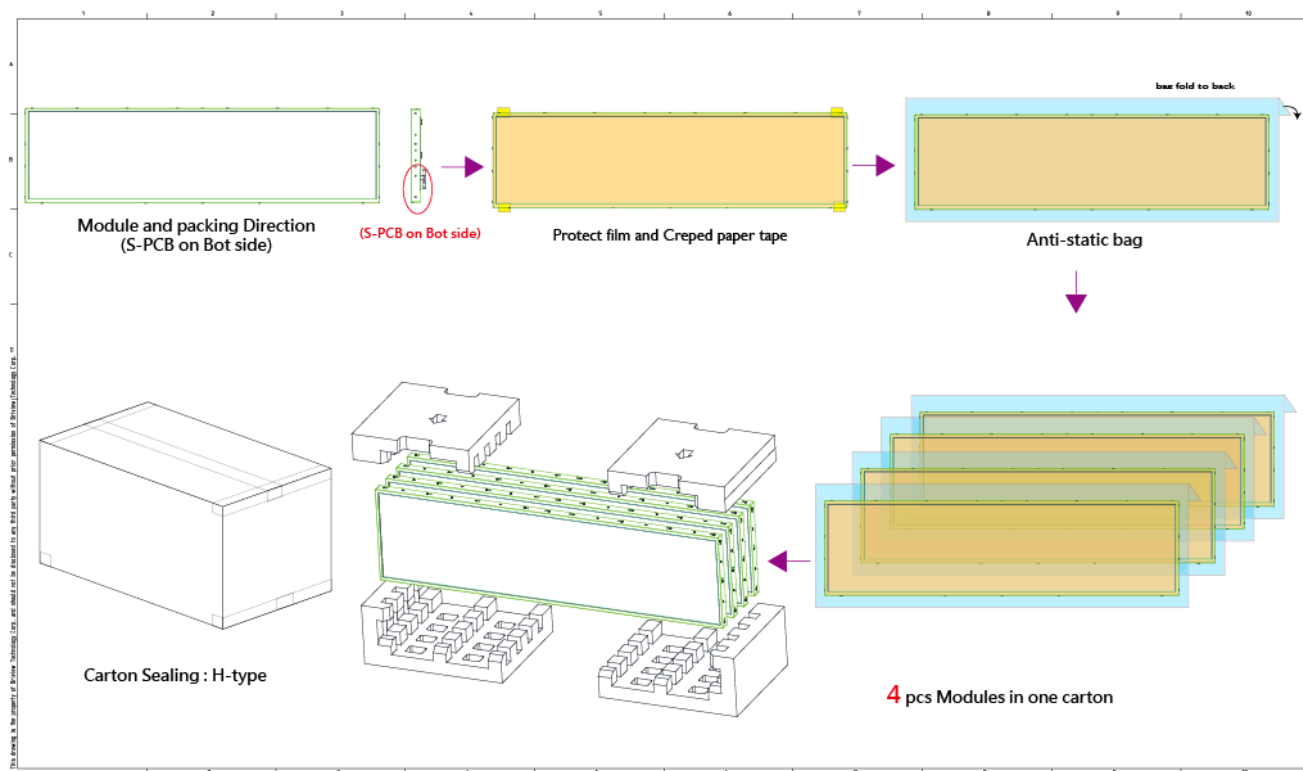
(2) For RoHs compatible products, AUO will add for identification.

Note: The green Mark will be present only when the green documents have been ready by AUO internal green team. (definition of green design follows the AUO green design checklist.)

#### B. Carton Label:

AU Optronics	QTY : 4		
MODEL NO: P420IVN03.1			
PART NO: 97.42P16.Xxx			
CUSTOMER NO:			
CARTON NO:			
Made in XXXXXX	*XXXXXX-XXXXXXXXXXXX*		

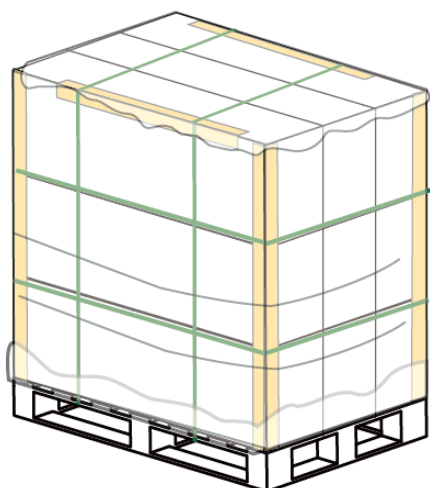
## 6-2 PACKING METHODS:



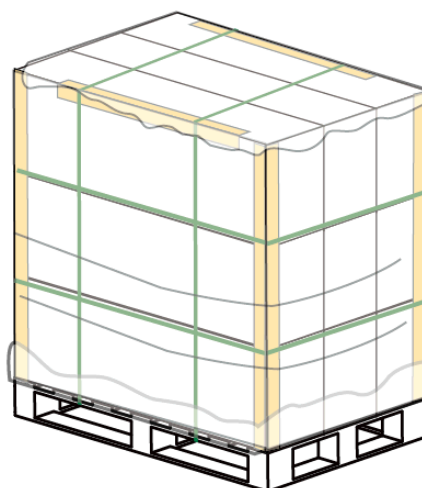


### 6-3 Pallet and Shipment Information

	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing Box	4pcs/box	1178(L)mm*375(W)mm*396(H)mm	25.4	
2	Pallet	1	1190(L)mm*1150(W)mm*132(H)mm	20	
3	Boxes per Pallet	9 boxes/Pallet (By Air) ; 9 Boxes/Pallet (By Sea)			
4	Panels per Pallet	36pcs/pallet(By Air) ; 36 pcs/Pallet (By Sea)			
5	Pallet after packing	36(by Air)	1190(L)mm*1150(W)mm*1320(H)mm (by Air)	248.6 (by Air)	
		36(by Sea)	1190(L)mm*1150(W)mm*1320(H)mm (by Sea)	248.6(by Sea)	40ft DC



Note:For Air Freight



Note:For 20'/40' DC & HQ Container

## 7. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

### 7-1 MOUNTING PRECAUTIONS

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit broken by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaked with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizer. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

### 7-2 OPERATING PRECAUTIONS

- (1) The device listed in the product specification sheets was designed and manufactured for PID application
- (2) The spike noise causes the miss-operation of circuits. It should be lower than following voltage:  
 $V = \pm 200\text{mV}$  (Over and under shoot voltage)
- (3) Response time depends on the temperature. (In lower temperature, it becomes longer..)
- (4) Brightness of LED depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.
- (5) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (6) When fixed patterns are displayed for a long time, remnant image is likely to occur.

- (7) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.

### **7.3 Operating Condition for Public Information Display**

The device listed in the product specification is designed and manufactured for PID (Public Information Display) application. To optimize module's lifetime and function, below operating usages are required.

(1) Normal operating condition

1. Operating temperature: 0~40°C
2. Operating humidity: 10~90%
3. Display pattern: dynamic pattern (Real display).

Note) Long-term static display would cause image sticking.

(3) Operation usage to protect against image sticking due to long-term static display.

- (1) Suitable operating time: 24 hours a day or less.

(\* The moving picture can be allowed for 24 hours a day)

- (2) Liquid Crystal refresh time is required. Cycling display between 5 minutes' information (static) display and 10 seconds' moving image.

- (3) Periodically change background and character (image) color.

- (4) Avoid combination of background and character with large different luminance.

(3) Periodically adopt one of the following actions after long time display.

- A. Running the screen saver (motion picture or black pattern)

- B. Power off the system for a while

- (4) LCD system is required to place in well-ventilated environment. Adapting active cooling system is highly recommended.

- (5) Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions, such as high temperature/ humidity, display stationary patterns, or long operation time etc..., it is strongly recommended to contact AUO for filed application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock market and controlling systems.

### **7.4 Electrostatic Discharge Control**

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

## **7.5 Precautions for Strong Light Exposure**

Strong light exposure causes degradation of polarizer and color filter.

## **7.6 Storage**

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.
- (3) Storage condition is guaranteed under packing conditions.
- (4) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition.

## **7.7 Handling Precautions for Protection Film**

- (1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
- (3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

## **7.8 Dust Resistance**

- (1) AUO module dust tests are conducted with marked areas (e.g., holes and slits around the front bezel and back cover) sealed, to comply with JIS D0207 (see Figure 1).
- (2) To prevent particles from entering the module, please ensure the set has all the highlighted areas (holes and slits) adequately sealed or covered by set mechanism.
- (3) AUO's testing procedure cannot replicate all real world operation scenarios. It is up to the module user to apply the most appropriate dust resistance solution for its particular application.

Figure 1

